Keysight D9040USBC USB4 Compliance Test Application

KEYSIGHT

METHODS OF IMPLEMENTATION

Notices

Trademarks

UNIX is a registered trademark of UNIX System Laboratories in the U.S.A. and other countries. Target is copyrighted by Thru-Put Systems, Inc.

Version

Version 1.30.0.0

Edition

January 2024

Available in electronic format only

Keysight Technologies, Inc.
1900 Garden of the Gods Road
Colorado Springs, CO 80907 USA

Warranty

THE MATERIAL CONTAINED IN THIS DOCUMENT IS PROVIDED "AS IS," AND IS SUBJECT TO BEING CHANGED, WITHOUT NOTICE, IN FUTURE EDITIONS. FURTHER, TO THE MAXIMUM EXTENT PERMITTED BY APPLICABLE LAW, KEYSIGHT DISCLAIMS ALL WARRANTIES, EITHER EXPRESS OR IMPLIED WITH REGARD TO THIS MANUAL AND ANY INFORMATION CONTAINED HEREIN, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. KEYSIGHT SHALL NOT BE LIABLE FOR ERRORS OR FOR INCIDENTAL OR CONSEQUENTIAL DAMAGES IN CONNECTION WITH THE FURNISHING, USE, OR PERFORMANCE OF THIS DOCUMENT OR ANY INFORMATION CONTAINED HEREIN. SHOULD KEYSIGHT AND THE USER HAVE A SEPARATE WRITTEN AGREEMENT WITH WARRANTY TERMS COVERING THE MATERIAL IN THIS DOCUMENT THAT CONFLICT WITH THESE TERMS, THE WARRANTY TERMS IN THE SEPARATE AGREEMENT WILL CONTROL.

Technology Licenses

The hardware and/or software described in this document are furnished under a license and may be used or copied only in accordance with the terms of such license.

U.S. Government Rights

The Software is "commercial computer software," as defined by Federal Acquisition Regulation ("FAR") 2.101. Pursuant to FAR 12.212 and 27.405-3 and Department of Defense FAR Supplement ("DFARS") 227.7202, the U.S. government acquires commercial computer software under the same terms by which the software is customarily provided to the public. Accordingly, Keysight provides the Software to U.S. government customers under its standard commercial license, which is embodied in its End User License Agreement (EULA), a copy of which can be found at http://www.keysight.com/find/sweula. The license set forth in the EULA represents the exclusive authority by which the U.S. government may use, modify, distribute, or disclose the Software. The EULA and the license set forth therein, does not require or permit, among other things, that Keysight: (1) Furnish technical information related to commercial computer software or commercial computer software documentation that is not customarily provided to the public; or (2) Relinquish to, or otherwise provide, the government rights in excess of these rights customarily provided to the public to use, modify, reproduce, release, perform, display, or disclose commercial computer software or commercial computer software documentation. No additional government requirements beyond those set forth in the EULA shall apply, except to the extent that those terms, rights, or licenses are explicitly required from all providers of commercial computer software pursuant to the FAR and the DFARS and are set forth specifically in writing elsewhere in the EULA. Keysight shall be under no obligation to update, revise or otherwise modify the Software. With respect to any technical data as defined by FAR 2.101, pursuant to FAR 12.211 and 27.404.2 and DFARS 227.7102, the U.S. government acquires no greater than Limited Rights as defined in FAR 27.401 or DFAR 227.7103-5 (c), as applicable in any technical data.

Safety Notices

CAUTION

A CAUTION notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in damage to the product or loss of important data. Do not proceed beyond a CAUTION notice until the indicated conditions are fully understood and met.

WARNING

A WARNING notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in personal injury or death. Do not proceed beyond a WARNING notice until the indicated conditions are fully understood and met.

Contents

1 Overview

USB4 Automated Testing–At a Glance 30

Required Equipment and Software 31

Hardware 31
Software 34
Licensing information 35

In This Book 36

See Also 36
References 36

2 Installing the Test Application and Licenses

Installing the Test Application 38

Installing the License Key 39

Using Keysight License Manager 5 39
Using Keysight License Manager 6 40

3 Preparing to Take Measurements

Calibrating the Oscilloscope 44

Starting the USB4 Test Application 45

Setting up the USB4 Test Application 48

Calibration Setup for Compliance Tests 56

Channel Skew Calibration 56
Preset Calibration 60
Power Profile 62
Fixture and Cable De-Embed 63

4 Host / Device USB4 Transmitter Testing

Architectural Overview 66

Overview 66
USB4 System Description 66

USB4 Electrical Compliance Methodology 68
System Compliance Test Point Definitions 68
Reference Clock-and-Data-Recovery (CDR) Function 69
Reference Equalization Function 70

Router Assembly Transmitter Compliance 73
Transmitter Specifications Applied for All Speeds 73
Transmitter Frequency Variations during Link Training 76
Transmitter Differential Return Loss 78
Transmitter Common Mode Return Loss 79
Transmit Equalization 80
Transmitter Compliance Specifications for Gen 2 83
Transmitter Compliance Specifications for Gen 3 Interconnects 85

5 Transmitter Tests for 10.3125 GB/s Systems

Tx Preset Calibration 91
Test Overview 91
Test Setup 91
Test Procedure 93
Expected / Observable Results 93
Test References 93

SBTX High Voltage 94
Test Overview 94
Test Pass Requirement 94
Test Procedure 94
Expected / Observable Results 95
Test References 95

SBTX Low Voltage 96
Test Overview 96
Test Pass Requirement 96
Test Procedure 96
Expected / Observable Results 97
Test References 97

SBTX Rise/Fall Time 98
Test Overview 98
Test Pass Requirement 98
Test Procedure 99
Expected / Observable Results 100
Test References 100

SBTX UI Duration 101
Test Overview 101
Test Pass Requirement 101
Test Procedure 102
Expected / Observable Results 103
Test References 103

SBRX High Voltage Detection 104
Test Overview 104
Test Pass Requirement 104
Test Procedure 105
Expected / Observable Results 105
Test References 105

SBRX Low Voltage Detection 106
Test Overview 106
Test Pass Requirement 106
Test Procedure 106
Expected / Observable Results 106
Test References 106

TX Rise/Fall Time 107
Test Overview 107
Test Pass Requirement 107
Test Setup 107
Test Procedure 108
Expected / Observable Results 108
Test References 108

Tx Uncorrelated Jitter 109
Test Overview 109
Test Pass Requirement 109
Test Setup 109
Test Procedure 110
Expected / Observable Results 110
Test References 110

Tx Uncorrelated Deterministic Jitter 111
Test Overview 111
Test Pass Requirement 111
Test Setup 111
Test Procedure 112
Expected / Observable Results 112
Test References 112

Tx Data Dependent Jitter 113
Test Overview 113
Test Pass Requirement 113
Test Setup 113
Test Procedure 114
Expected / Observable Results 114
Test References 114

Tx Duty Cycle Distortion 115
Test Overview 115
Test Pass Requirement 115
Test Setup 115
Test Procedure 116
Expected / Observable Results 116
Test References 116

Tx Low Frequency Uncorrelated Deterministic Jitter 117
Test Overview 117
Test Pass Requirement 117
Test Setup 117
Test Procedure 118
Expected / Observable Results 118
Test References 118

Tx Total Jitter 119
Test Overview 119
Test Pass Requirement 119
Test Setup 119
Test Procedure 120
Expected / Observable Results 120
Test References 120

Tx Uncorrelated Jitter TP3 121
Test Overview 121
Test Pass Requirement 121
Test Setup 121
Test Procedure 122
Expected / Observable Results 122
Test References 122

Tx Uncorrelated Deterministic Jitter TP3 123
Test Overview 123
Test Pass Requirement 123
Test Setup 123
Test Procedure 124
Expected / Observable Results 124
Test References 124

Tx Total Jitter TP3 125
Test Overview 125
Test Pass Requirement 125
Test Setup 125
Test Procedure 126
Expected / Observable Results 126
Test References 127

Tx Eye Diagram TP3 128
Test Overview 128
Test Pass Requirement 128
Test Setup 129
Test Procedure 130
Expected / Observable Results 130
Test References 130

Tx Average Unit Interval, Min/Max 131
Test Overview 131
Test Pass Requirement 131
Test Setup 131
Test Procedure 132
Expected / Observable Results 132
Test References 132

Tx Minimum Unit Interval, Min/Max 133
Test Overview 133
Test Pass Requirement 133
Test Setup 133
Test Procedure 134
Expected / Observable Results 134
Test References 134

Tx SSC Down Spread Rate 135
Test Overview 135
Test Pass Requirement 135
Test Setup 135
Test Procedure 136
Expected / Observable Results 136
Test References 136

Tx SSC Down Spread Range 137
Test Overview 137
Test Pass Requirement 137
Test Setup 137
Test Procedure 138
Expected / Observable Results 138
Test References 138

Tx SSC Slew Rate 139
Test Overview 139
Test Pass Requirement 139
Test Setup 139
Test Procedure 140
Expected / Observable Results 140
Test References 140

Tx SSC Phase Deviation 141
Test Overview 141
Test Pass Requirement 141
Test Setup 141
Test Procedure 142
Expected / Observable Results 142
Test References 142

Tx Eye Diagram 143
Test Overview 143
Test Pass Requirement 143
Test Setup 143
Test Procedure 144
Expected / Observable Results 144
Test References 145

Tx AC Common Mode Voltage 146
Test Overview 146
Test Pass Requirement 146
Test Setup 146
Test Procedure 147
Expected / Observable Results 147
Test References 147

Tx Equalization Tests 148
Test Overview 148
Test Pass Requirement 148
Test Setup 149
Test Procedure 151
Expected / Observable Results 153
Test References 153

Tx Electrical Idle Voltage Test 154
Test Overview 154
Test Pass Requirement 154
Test Setup 154
Test Procedure 155
Measurement Procedure 155
Expected / Observable Results 155
Test References 155

Tx Differential Return Loss Test 156
Test Overview 156
Test Pass Requirement 156
Test Setup 157
Test Procedure 160
Expected / Observable Results 160
Test References 160

Tx Common Mode Return Loss Test 161
Test Overview 161
Test Pass Requirement 161
Test Setup 162
Test Procedure 165
Expected / Observable Results 165
Test References 165

Rx Differential Return Loss Test 166
Test Overview 166
Test Pass Requirement 166
Test Setup 167
Test Procedure 170
Expected / Observable Results 170
Test References 170

Rx Common Mode Return Loss Test 171
Test Overview 171
Test Pass Requirement 171
Test Setup 172
Test Procedure 175
Expected / Observable Results 175
Test References 175

6 Transmitter Tests for 10 GB/s Systems

Tx Preset Calibration 178
Test Overview 178
Test Setup 178
Test Procedure 181
Expected / Observable Results 181
Test References 181

SBTX High Voltage 182
Test Overview 182
Test Pass Requirement 182
Test Procedure 182
Expected / Observable Results 183
Test References 183

SBTX Low Voltage 184
Test Overview 184
Test Pass Requirement 184
Test Procedure 184
Expected / Observable Results 185
Test References 185

SBTX Rise/Fall Time 186
Test Overview 186
Test Pass Requirement 186
Test Procedure 187
Expected / Observable Results 188
Test References 188

SBTX UI Duration 189
Test Overview 189
Test Pass Requirement 189
Test Procedure 190
Expected / Observable Results 191
Test References 191

SBRX High Voltage Detection 192
Test Overview 192
Test Pass Requirement 192
Test Procedure 193
Expected / Observable Results 193
Test References 193

SBRX Low Voltage Detection 194
Test Overview 194
Test Pass Requirement 194
Test Procedure 194
Expected / Observable Results 194
Test References 194

Tx Rise/Fall Time 195
Test Overview 195
Test Pass Requirement 195
Test Setup 195
Test Procedure 196
Expected / Observable Results 196
Test References 196

Tx Uncorrelated Jitter 197
Test Overview 197
Test Pass Requirement 197
Test Setup 197
Test Procedure 198
Expected / Observable Results 198
Test References 198

Tx Uncorrelated Deterministic Jitter 199
Test Overview 199
Test Pass Requirement 199
Test Setup 199
Test Procedure 200
Expected / Observable Results 200
Test References 200

Tx Data Dependent Jitter 201
Test Overview 201
Test Pass Requirement 201
Test Setup 201
Test Procedure 202
Expected / Observable Results 202
Test References 202

Tx Duty Cycle Distortion 203
Test Overview 203
Test Pass Requirement 203
Test Setup 203
Test Procedure 204
Expected / Observable Results 204
Test References 204

Tx Low Frequency Uncorrelated Deterministic Jitter 205
Test Overview 205
Test Pass Requirement 205
Test Setup 205
Test Procedure 206
Expected / Observable Results 206
Test References 206

Tx Total Jitter 207
Test Overview 207
Test Pass Requirement 207
Test Setup 207
Test Procedure 208
Expected / Observable Results 208
Test References 208

Tx Uncorrelated Jitter TP3 209
Test Overview 209
Test Pass Requirement 209
Test Setup 209
Test Procedure 210
Expected / Observable Results 210
Test References 210

Tx Uncorrelated Deterministic Jitter TP3 211
Test Overview 211
Test Pass Requirement 211
Test Setup 211
Test Procedure 212
Expected / Observable Results 212
Test References 212

Tx Total Jitter TP3 213
Test Overview 213
Test Pass Requirement 213
Test Setup 213
Test Procedure 214
Expected / Observable Results 214
Test References 215

Tx Eye Diagram TP3 216
Test Overview 216
Test Pass Requirement 216
Test Setup 216
Test Procedure 217
Expected / Observable Results 217
Test References 218

Tx Minimum Unit Interval, Min/Max 219
Test Overview 219
Test Pass Requirement 219
Test Setup 219
Test Procedure 220
Expected / Observable Results 220
Test References 220

Tx SSC Down Spread Rate 221
Test Overview 221
Test Pass Requirement 221
Test Setup 221
Test Procedure 222
Expected / Observable Results 222
Test References 222

Tx SSC Down Spread Range 223
Test Overview 223
Test Pass Requirement 223
Test Setup 223
Test Procedure 224
Expected / Observable Results 224
Test References 224
Tx SSC Slew Rate 225
Test Overview 225
Test Pass Requirement 225
Test Setup 225
Test Procedure 226
Expected / Observable Results 226
Test References 226
Tx SSC Phase Deviation 227
Test Overview 227
Test Pass Requirement 227
Test Setup 227
Test Procedure 228
Expected / Observable Results 228
Test References 228
Tx Eye Diagram 229
Test Overview 229
Test Pass Requirement 229
Test Setup 229
Test Procedure 230
Expected / Observable Results 230
Test References 230
Tx AC Common Mode Voltage 231
Test Overview 231
Test Pass Requirement 231
Test Setup 231
Test Procedure 232
Expected / Observable Results 232
Test References 232

Tx Equalization Tests 233
Test Overview 233
Test Pass Requirement 233
Test Setup 234
Test Procedure 235
Expected / Observable Results 237
Test References 237

Tx Electrical Idle Voltage Test 238
Test Overview 238
Test Pass Requirement 238
Test Setup 238
Test Procedure 239
Measurement Procedure 239
Expected / Observable Results 239
Test References 239

Tx Differential Return Loss Test 240
Test Overview 240
Test Pass Requirement 240
Test Setup 241
Test Procedure 244
Expected / Observable Results 244
Test References 244

Tx Common Mode Return Loss Test 245
Test Overview 245
Test Pass Requirement 245
Test Setup 246
Test Procedure 249
Expected / Observable Results 249
Test References 249

Rx Differential Return Loss Test 250
Test Overview 250
Test Pass Requirement 250
Test Setup 251
Test Procedure 254
Expected / Observable Results 254
Test References 254

Rx Common Mode Return Loss Test 255
Test Overview 255
Test Pass Requirement 255
Test Setup 256
Test Procedure 259
Expected / Observable Results 259
Test References 259

7 Transmitter Tests for 20.625 GB/s Systems

Tx Preset Calibration 262
Test Overview 262
Test Setup 262
Test Procedure 265
Expected / Observable Results 265
Test References 265

SBTX High Voltage 266
Test Overview 266
Test Pass Requirement 266
Test Procedure 266
Expected / Observable Results 267
Test References 267

SBTX Low Voltage 268
Test Overview 268
Test Pass Requirement 268
Test Procedure 268
Expected / Observable Results 269
Test References 269

SBTX Rise/Fall Time 270
Test Overview 270
Test Pass Requirement 270
Test Procedure 271
Expected / Observable Results 272
Test References 272

SBTX UI Duration 273
Test Overview 273
Test Pass Requirement 273
Test Procedure 274
Expected / Observable Results 275
Test References 275

SBRX High Voltage Detection 276
Test Overview 276
Test Pass Requirement 276
Test Procedure 277
Expected / Observable Results 277
Test References 277

SBRX Low Voltage Detection 278
Test Overview 278
Test Pass Requirement 278
Test Procedure 278
Expected / Observable Results 278
Test References 278

Tx Rise/Fall Time 279
Test Overview 279
Test Pass Requirement 279
Test Setup 279
Test Procedure 280
Expected / Observable Results 280
Test References 280

Tx Uncorrelated Jitter 281
Test Overview 281
Test Pass Requirement 281
Test Setup 281
Test Procedure 282
Expected / Observable Results 282
Test References 282

Tx Uncorrelated Deterministic Jitter 283
Test Overview 283
Test Pass Requirement 283
Test Setup 283
Test Procedure 284
Expected / Observable Results 284
Test References 284

Tx Data Dependent Jitter 285
Test Overview 285
Test Pass Requirement 285
Test Setup 285
Test Procedure 286
Expected / Observable Results 286
Test References 286

Tx Duty Cycle Distortion 287
Test Overview 287
Test Pass Requirement 287
Test Setup 287
Test Procedure 288
Expected / Observable Results 288
Test References 288

Tx Low Frequency Uncorrelated Deterministic Jitter 289
Test Overview 289
Test Pass Requirement 289
Test Setup 289
Test Procedure 290
Expected / Observable Results 290
Test References 290

Tx Total Jitter 291
Test Overview 291
Test Pass Requirement 291
Test Setup 291
Test Procedure 292
Expected / Observable Results 292
Test References 292

Tx Uncorrelated Jitter TP3 293
Test Overview 293
Test Pass Requirement 293
Test Setup 293
Test Procedure 294
Expected / Observable Results 294
Test References 294

Tx Uncorrelated Deterministic Jitter TP3 295
Test Overview 295
Test Pass Requirement 295
Test Setup 295
Test Procedure 296
Expected / Observable Results 296
Test References 296

Tx Total Jitter TP3 297
Test Overview 297
Test Pass Requirement 297
Test Setup 297
Test Procedure 298
Expected / Observable Results 299
Test References 299

Tx Eye Diagram TP3 300
Test Overview 300
Test Pass Requirement 300
Test Setup 300
Test Procedure 301
Expected / Observable Results 302
Test References 302

Tx Minimum Unit Interval Min/Max 303
Test Overview 303
Test Pass Requirement 303
Test Setup 303
Test Procedure 304
Expected / Observable Results 304
Test References 304

Tx SSC Down Spread Rate 305
Test Overview 305
Test Pass Requirement 305
Test Setup 305
Test Procedure 306
Expected / Observable Results 306
Test References 306

Tx SSC Down Spread Range 307
Test Overview 307
Test Pass Requirement 307
Test Setup 307
Test Procedure 308
Expected / Observable Results 308
Test References 308

Tx SSC Slew Rate 309
Test Overview 309
Test Pass Requirement 309
Test Setup 309
Test Procedure 310
Expected / Observable Results 310
Test References 310
Tx SSC Phase Deviation 311
Test Overview 311
Test Pass Requirement 311
Test Setup 311
Test Procedure 312
Expected / Observable Results 312
Test References 312
Tx Eye Diagram 313
Test Overview 313
Test Pass Requirement 313
Test Setup 313
Test Procedure 314
Expected / Observable Results 314
Test References 315
Tx AC Common Mode Voltage 316
Test Overview 316
Test Pass Requirement 316
Test Setup 316
Test Procedure 317
Expected / Observable Results 317
Test References 317
Tx Equalization Tests 318
Test Overview 318
Test Pass Requirement 318
Test Setup 319
Test Procedure 320
Expected / Observable Results 322
Test References 322

Tx Electrical Idle Voltage Test 323
Test Overview 323
Test Pass Requirement 323
Test Setup 323
Test Procedure 324
Measurement Procedure 324
Expected / Observable Results 324
Test References 324
Tx Differential Return Loss Test 325
Test Overview 325
Test Pass Requirement 325
Test Setup 326
Test Procedure 329
Expected / Observable Results 329
Test References 329
Tx Common Mode Return Loss Test 330
Test Overview 330
Test Pass Requirement 330
Test Setup 331
Test Procedure 334
Expected / Observable Results 334
Test References 334
Rx Differential Return Loss Test 335
Test Overview 335
Test Pass Requirement 335
Test Setup 336
Test Procedure 339
Expected / Observable Results 339
Test References 339
Rx Common Mode Return Loss Test 340
Test Overview 340
Test Pass Requirement 340
Test Setup 341
Test Procedure 344
Expected / Observable Results 344
Test References 344

8 Transmitter Tests for 20 GB/s Systems

Tx Preset Calibration 347
- Test Overview 347
- Test Setup 347
- Test Procedure 349
- Expected / Observable Results 349
- Test References 349

SBTX High Voltage 350
- Test Overview 350
- Test Pass Requirement 350
- Test Procedure 350
- Expected / Observable Results 351
- Test References 351

SBTX Low Voltage 352
- Test Overview 352
- Test Pass Requirement 352
- Test Procedure 352
- Expected / Observable Results 353
- Test References 353

SBTX Rise/Fall Time 354
- Test Overview 354
- Test Pass Requirement 354
- Test Procedure 355
- Expected / Observable Results 356
- Test References 356

SBTX UI Duration 357
- Test Overview 357
- Test Pass Requirement 357
- Test Procedure 358
- Expected / Observable Results 359
- Test References 359

SBRX High Voltage Detection 360
- Test Overview 360
- Test Pass Requirement 360
- Test Procedure 361
- Expected / Observable Results 361
- Test References 361

SBRX Low Voltage Detection 362
Test Overview 362
Test Pass Requirement 362
Test Procedure 362
Expected / Observable Results 362
Test References 362

Tx Rise/Fall Time 363
Test Overview 363
Test Pass Requirement 363
Test Setup 363
Test Procedure 364
Expected / Observable Results 364
Test References 364

Tx Uncorrelated Jitter 365
Test Overview 365
Test Pass Requirement 365
Test Setup 365
Test Procedure 366
Expected / Observable Results 366
Test References 366

Tx Uncorrelated Deterministic Jitter 367
Test Overview 367
Test Pass Requirement 367
Test Setup 367
Test Procedure 368
Expected / Observable Results 368
Test References 368

Tx Data Dependent Jitter 369
Test Overview 369
Test Pass Requirement 369
Test Setup 369
Test Procedure 370
Expected / Observable Results 370
Test References 370

Tx Duty Cycle Distortion 371
Test Overview 371
Test Pass Requirement 371
Test Setup 371
Test Procedure 372
Expected / Observable Results 372
Test References 372

Tx Low Frequency Uncorrelated Deterministic Jitter 373
Test Overview 373
Test Pass Requirement 373
Test Setup 373
Test Procedure 374
Expected / Observable Results 374
Test References 374

Tx Total Jitter 375
Test Overview 375
Test Pass Requirement 375
Test Setup 375
Test Procedure 376
Expected / Observable Results 376
Test References 376

Tx Uncorrelated Jitter TP3 377
Test Overview 377
Test Pass Requirement 377
Test Setup 377
Test Procedure 378
Expected / Observable Results 378
Test References 378

Tx Uncorrelated Deterministic Jitter TP3 379
Test Overview 379
Test Pass Requirement 379
Test Setup 379
Test Procedure 380
Expected / Observable Results 380
Test References 380

Tx Total Jitter TP3 381
Test Overview 381
Test Pass Requirement 381
Test Setup 381
Test Procedure 382
Expected / Observable Results 383
Test References 383

Tx Eye Diagram TP3 384
Test Overview 384
Test Pass Requirement 384
Test Setup 384
Test Procedure 385
Expected / Observable Results 386
Test References 386

Tx Minimum Unit Interval, Min/Max 387
Test Overview 387
Test Pass Requirement 387
Test Setup 387
Test Procedure 388
Expected / Observable Results 388
Test References 388

Tx SSC Down Spread Rate 389
Test Overview 389
Test Pass Requirement 389
Test Setup 389
Test Procedure 390
Expected / Observable Results 390
Test References 390

Tx SSC Down Spread Range 391
Test Overview 391
Test Pass Requirement 391
Test Setup 391
Test Procedure 392
Expected / Observable Results 392
Test References 392

Tx SSC Slew Rate 393
Test Overview 393
Test Pass Requirement 393
Test Setup 393
Test Procedure 394
Expected / Observable Results 394
Test References 394

Tx SSC Phase Deviation 395
Test Overview 395
Test Pass Requirement 395
Test Setup 395
Test Procedure 396
Expected / Observable Results 396
Test References 396
Tx Eye Diagram 397
Test Overview 397
Test Pass Requirement 397
Test Setup 397
Test Procedure 398
Expected / Observable Results 398
Test References 399
Tx AC Common Mode Voltage 400
Test Overview 400
Test Pass Requirement 400
Test Setup 400
Test Procedure 401
Expected / Observable Results 401
Test References 401
Tx Equalization Tests 402
Test Overview 402
Test Pass Requirement 402
Test Setup 403
Test Procedure 404
Expected / Observable Results 406
Test References 406
Tx Electrical Idle Voltage Test 407
Test Overview 407
Test Pass Requirement 407
Test Setup 407
Test Procedure 408
Measurement Procedure 408
Expected / Observable Results 408
Test References 408

Tx Differential Return Loss Test 409
Test Overview 409
Test Pass Requirement 409
Test Setup 410
Test Procedure 413
Expected / Observable Results 413
Test References 413
Tx Common Mode Return Loss Test 414
Test Overview 414
Test Pass Requirement 414
Test Setup 415
Test Procedure 418
Expected / Observable Results 418
Test References 418
Rx Differential Return Loss Test 419
Test Overview 419
Test Pass Requirement 419
Test Setup 420
Test Procedure 423
Expected / Observable Results 423
Test References 423
Rx Common Mode Return Loss Test 424
Test Overview 424
Test Pass Requirement 424
Test Setup 425
Test Procedure 428
Expected / Observable Results 428
Test References 428
Index

1 Overview

USB4 Automated Testing—At a Glance 30
Required Equipment and Software 31
In This Book 36

USB4 Automated Testing—At a Glance

The Keysight D9040USBC USB4 Compliance Test Application allows the testing of all the 3rd Generation USB devices with the Keysight Infiniium Oscilloscope. These tests are based on the *Universal Serial Bus 4 (USB4®) Specification, Revision 2.0*.

The USB Type-C connector in conjunction with a USB Controller is capable of providing two dual-simplex lanes (or channels). Each lane provides bi-directional 10.3125 GB/s, 20.625 GB/s, 10 GB/s, or 20 GB/s of bandwidth. The USB Type-C connector is capable of connecting USB products when using either a USB Type-C Full Featured cable, a USB Passive cable, a USB Active Electrical or Optical cable, or USB legacy cable or dongle.

The USB4 Test Application:

- Lets you select individual or multiple tests to run.
- Lets you identify the device being tested and its configuration.
- Shows you how to make oscilloscope connections to the device under test.
- Automatically checks for proper oscilloscope configuration.
- Automatically sets up the oscilloscope for each test.
- Provides detailed information for each test that has been run, and lets you specify the thresholds at which marginal or critical warnings appear.
- Creates a printable HTML report of the tests that have been run.

NOTE The tests performed by the USB4 Test Application are intended to provide a quick check of the electrical health of the DUT. This testing is not a replacement for an exhaustive test validation plan.

NOTE Keysight D9040USBC USB4 Compliance Test Application supports ;D9010AGGC Compliance Test Software Measurement Server for using multiple machines/PCs over a network as acquisition engines and processing engines in order to significantly enhance the test execution speed. To know more, please see the D9010AGGC product page on keysight.com.

Required Equipment and Software

In order to run the USB4 automated tests, you need the following equipment and software:

Hardware

- Use one of the Oscilloscope models given in Table 1.
- Keyboard, qty = 1, (provided with the Keysight Infiniium oscilloscope)
- Mouse, qty = 1, (provided with the Keysight Infiniium oscilloscope)
- Keysight also recommends using a second monitor to view the test application.

Table 1 lists the recommended test equipments for running the USB4 tests. Note that all test equipments require Calibration to ensure accurate and repeatable results. The test equipments must be calibrated prior to, and if necessary, during the test procedure.

Table 1 Test Equipments and Accessories for USB4 Tests

Required Equipment	Test Equipment Capabilities/Description	Recommended Test Equipment
Test Point Access Boards	TPA Boards provide test point for the pins on the USB connector and an easy way to control the DUT.	▪ USB Plug Test Fixture or equivalent ▪ Wilder TBT-TPA-UHG2 TBT/USB4 Micro-Controller Test Module with USB Cable or equivalent ▪ Wilder USB4-TPA-UC USB4 Micro-Controller Test Module with USB Cable (Type A to Type B)

Required Equipment	Test Equipment Capabilities/Description	Recommended Test Equipment
Real Time Scopes (choose from one of the available options)	▪ DC to 21±1GHz -3dB bandwidth or greater ▪ 80G sample/sec Sampling rate or greater, sampling 2 channels simultaneously ▪ Sample memory: 2 channels at 50M samples per channel or greater ▪ 1st and 2nd order CDR capability ▪ Equalization for USB 3.1 model capability	▪ Keysight Z-Series Oscilloscope (25GHz and above)
	▪ DC to 21±1GHz -3dB bandwidth or greater ▪ 128G sample/sec Sampling rate or greater, sampling 2 channels simultaneously ▪ Sample memory: 2 channels at 50M samples per channel or greater ▪ 1st and 2nd order CDR capability ▪ Equalization for USB 3.1 model capability	▪ Keysight UXR Series Oscilloscope (25GHz and above)
	▪ DC to 21±1GHz -3dB bandwidth or greater ▪ 80G sample/sec Sampling rate or greater, sampling 2 channels simultaneously ▪ Sample memory: 2 channels at 50M samples per channel or greater ▪ 1st and 2nd order CDR capability ▪ Equalization for USB 3.1 model capability	▪ Keysight V-Series Oscilloscope (25GHz and above)
	▪ DC to 21±1GHz -3dB bandwidth or greater ▪ 80G sample/sec Sampling rate or greater, sampling 2 channels simultaneously ▪ Sample memory: 2 channels at 50M samples per channel or greater ▪ 1st and 2nd order CDR capability ▪ Equalization for USB 3.1 model capability	▪ Keysight Q-Series Oscilloscope (25GHz and above)
Accessories		
Low insertion loss phase matched cables	▪ Phase matched ±2° @ 40GHz ▪ Max IL in 10GHz < 1.2dB	▪ Rosenberger UK Micro Coax FC142A0-014-MTIE 2.92m (x2) L-1m (40GHz) ▪ Rosenberger Adaptor: RPC-2.92 female – SMP female - 02K119-K00E3

VNA Configuration Requirements

Required Equipment	Equipment Description	Qty

Network Analyzer	Keysight Vector Network Analyzer:
	▪ 20 GHz is recommended as USB4 requires measurements up to 20 GHz.
	▪ Minimum 4-Port VNA to support USB4 SigTest tool requirement.
	  ▪ E5080B-4K0: 4-port test set, 9 kHz to 20 GHz or
	  ▪ P5024A-400 Streamline USB Series VNA or
	  ▪ M9804A-400 PXI Multiport VNA or
	  ▪ N522xB 4-Port PNA
	
	Note 1:
	Ensure that the VNA firmware revision is A.17.25.05 or higher to be compatible with the return loss test automation.
	(Windows 10)
	
	Note 2:
	All 2-Port VNA and legacy E5071C will not be supported. Please refer to Return Loss Test MOI for manual setup.
		1 each

ECal Module	4-Port Electronic Calibration (ECal) Module ▪ N4433D-010/0DC 4-Ports	1 each

Software

- The minimum version of Infiniium oscilloscope software (see the Keysight D9040USBC USB4 Compliance Test Application Release Notes)
- Keysight D9040USBC USB4 Compliance Test Application software
- SigTest setup software list:
  - Matlab runtime compiler MCR R2021b (9.11)
  - USB4 SigTest tool
  - USB4 ETT tool
  - Wilder USB4 microcontroller USB drivers
  - Wilder USB4 microcontroller UI executable
  - FTDI chip driver

NOTE For more information on SigTest setup, please see **Keysight D9040USBC USB4 Compliance Test Application Online Help > Setting Up the Test Environment > SigTest Setup**.

Licensing information

Refer to the *Data Sheet* pertaining to USB4 Test Application to know about the licenses you must install along with other optional licenses. Visit "http://www.keysight.com/find/D9040USBC" and in the web page's **Resources** tab, you may view the associated Data Sheet.

To procure a license, you require the Host ID information that is displayed in the Keysight License Manager application installed on the same machine where you wish to install the license.

The licensing format for Keysight License Manager 6 differs from its predecessors. See "Installing the License Key" on page 39 to see the difference in installing a license key using either of the applications on your machine.

In This Book

This manual describes the tests that are performed by the USB4 Test Application in more detail.

- Chapter 2, “Installing the Test Application and Licenses” describes how to install the software and licenses for the USB4 Test Application software (if it was purchased separately).
- Chapter 3, “Preparing to Take Measurements” describes how to start the USB4 Test Application and gives a brief overview of its features.
- Chapter 4, “Host / Device USB4 Transmitter Testing” contains an overview on the USB system components and requirements for Transmitter testing.
- Chapter 5, “Transmitter Tests for 10.3125 GB/s Systems” describes procedures to run electrical tests on a USB DUT operating at a bit rate of 10.3125 GB/s.
- Chapter 6, “Transmitter Tests for 10 GB/s Systems” describes procedures to run electrical tests on a USB DUT operating at a rounded-off bit rate of 10 GB/s.
- Chapter 7, “Transmitter Tests for 20.625 GB/s Systems” describes procedures to run electrical tests on a USB DUT operating at a bit rate of 20.625 GB/s.
- Chapter 8, “Transmitter Tests for 20 GB/s Systems” describes procedures to run electrical tests on a USB DUT operating at a rounded-off bit rate of 20 GB/s.

See Also

The Keysight D9040USBC USB4 Compliance Test Application’s Online Help, which describes:

- Starting the USB4 Test Application
- Creating or Opening a Test Project
- Setting Up the Test Environment
- Selecting Tests
- Configuring Tests
- Verifying Physical Connections
- Running Tests
- Configuring Automation in the Test Application
- Viewing Results
- Viewing HTML Test Report
- Exiting the Test Application
- Additional Settings in the Test App

References

- The USB standard specifications are available in Universal Serial Bus 4 (USB4™) Specification Version 1.0.

2 Installing the Test Application and Licenses

Installing the Test Application / 38
Installing the License Key / 39

If you purchased the Keysight D9040USBC USB4 Compliance Test Application separate from your Infiniium oscilloscope, you must install the software and license key.

NOTE For information on SigTest setup, please see **Keysight D9040USBC USB4 Compliance Test Application Online Help > Setting Up the Test Environment > SigTest Setup**.

Installing the Test Application

1. Make sure you have the minimum version of Infiniium Oscilloscope software (see the D9040USBC USB4 Test Application release notes). To ensure that you have the minimum version, select **Help > About Infiniium...** from the main menu.
2. To obtain the USB4 Test Application, go to Keysight website: "http://www.keysight.com/find/D9040USBC".
3. In the web page's **Trials & Licenses** tab, click the **Details and Download** button to view instructions for downloading and installing the application software.

Installing the License Key

To procure a license, you require the Host ID information that is displayed in the Keysight License Manager application installed on the same machine where you wish to install the license.

Using Keysight License Manager 5

To view and copy the Host ID from Keysight License Manager 5:

1 Launch Keysight License Manager on your machine, where you wish to run the Test Application and its features.

2 Copy the Host ID that appears on the top pane of the application. Note that x indicates numeric values.

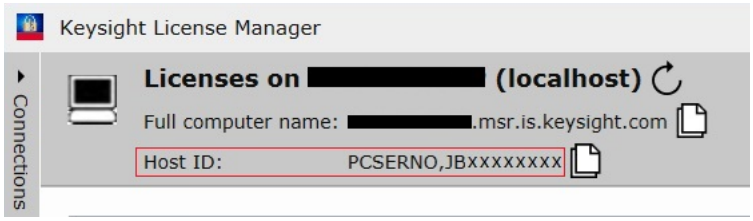


Figure 1 Viewing the Host ID information in Keysight License Manager 5

To install one of the procured licenses using Keysight License Manager 5 application,

1 Save the license files on the machine, where you wish to run the Test Application and its features.

2 Launch Keysight License Manager.

3 From the configuration menu, use one of the options to install each license file.

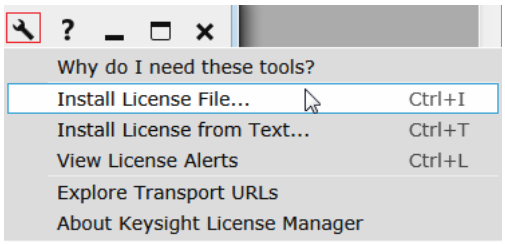


Figure 2 Configuration menu options to install licenses on Keysight License Manager 5

For more information regarding installation of procured licenses on Keysight License Manager 5, refer to Keysight License Manager 5 Supporting Documentation.

Using Keysight License Manager 6

To view and copy the Host ID from Keysight License Manager 6:

1. Launch Keysight License Manager 6 on your machine, where you wish to run the Test Application and its features.
2. Copy the Host ID, which is the first set of alphanumeric value (as highlighted in Figure 3) that appears in the Environment tab of the application. Note that x indicates numeric values.

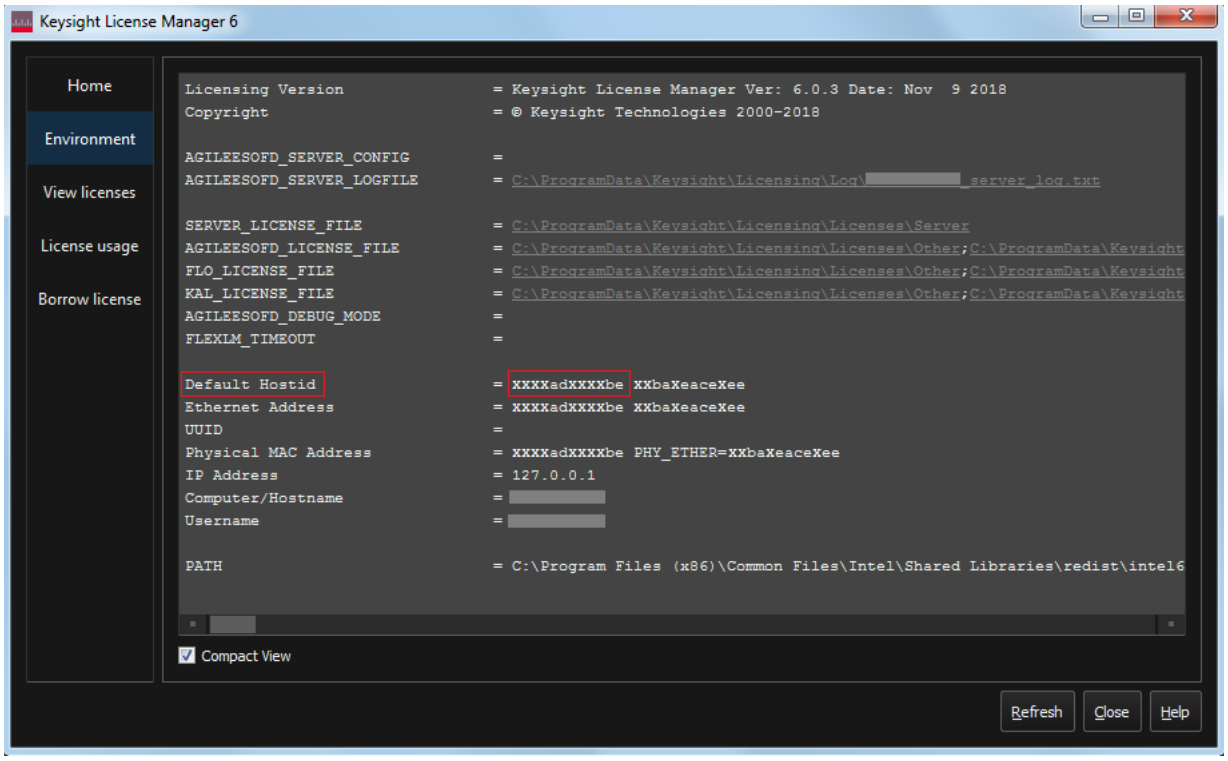


Figure 3 Viewing the Host ID information in Keysight License Manager 6

To install one of the procured licenses using Keysight License Manager 6 application,

1 Save the license files on the machine, where you wish to run the Test Application and its features.

2 Launch Keysight License Manager 6.

3 From the Home tab, use one of the options to install each license file.

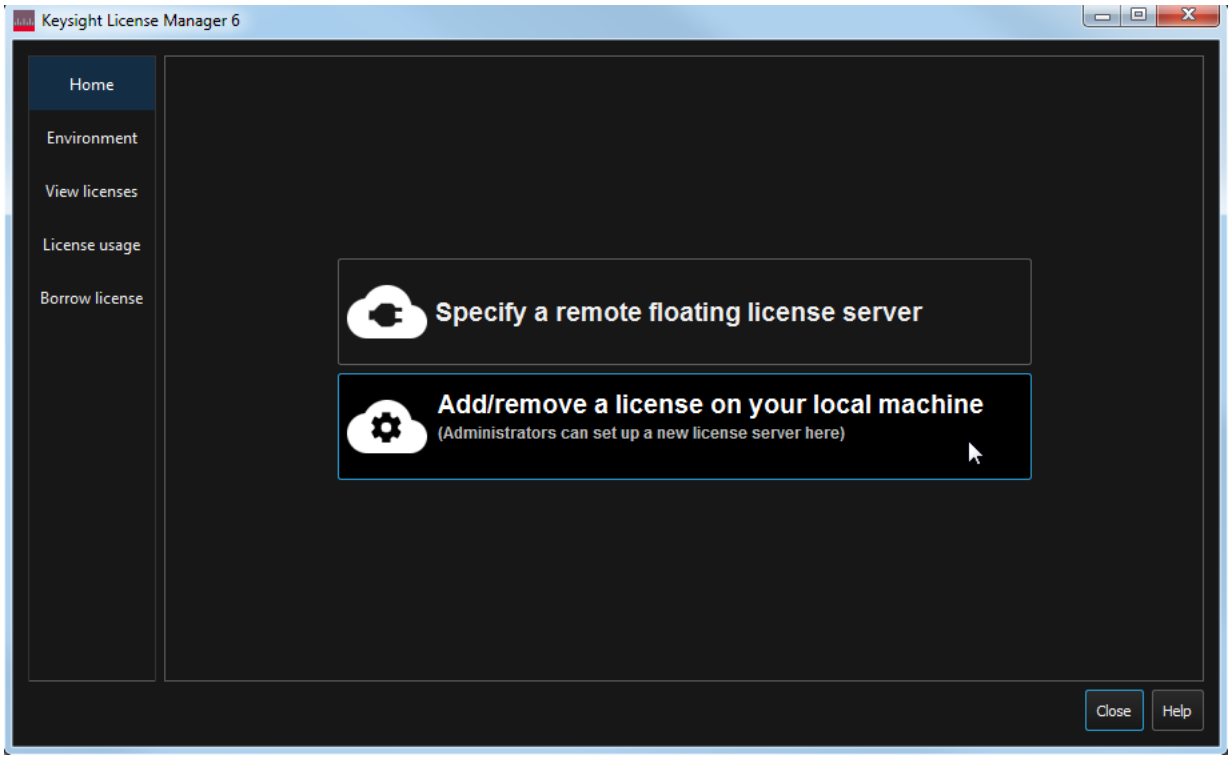


Figure 4 Home menu options to install licenses on Keysight License Manager 6

For more information regarding installation of procured licenses on Keysight License Manager 6, refer to Keysight License Manager 6 Supporting Documentation.

3 Preparing to Take Measurements

Calibrating the Oscilloscope / 44
Starting the USB4 Test Application / 45
Setting up the USB4 Test Application / 48
Calibration Setup for Compliance Tests / 56

Before running the automated tests, you should calibrate the oscilloscope. After the oscilloscope has been calibrated, you are ready to start the USB4 Test Application and perform the measurements.

NOTE For information on SigTest setup, please see **Keysight D9040USBC USB4 Compliance Test Application Online Help > Setting Up the Test Environment > SigTest Setup**.

Calibrating the Oscilloscope

If you have not already calibrated the oscilloscope, refer to the *User Guide* for the respective Oscilloscope you are using.

NOTE If the ambient temperature changes more than 5 degrees Celsius from the Calibration temperature, internal Calibration should be performed again. The delta between the Calibration temperature and the present operating temperature is shown in the **Utilities > Calibration** menu.

NOTE If you switch cables between channels or other Oscilloscopes, it is necessary to perform cable and probe Calibration again. Keysight recommends that, once Calibration is performed, you label the cables with the channel on which they were calibrated.

Starting the USB4 Test Application

1 Ensure that the USB4 Device Under Test (DUT) is operating and set to desired test modes. To start the USB4 Test Application: From the Infiniium Oscilloscope's main menu, select **Analyze > Automated Test Apps > D9040USBC USB4 Test App**

NOTE The **Test Lane** drop-down options in the **Set Up** tab, when the Test App is launched on a 4-Channel Oscilloscope, are different from that on a 2-Channel Oscilloscope.

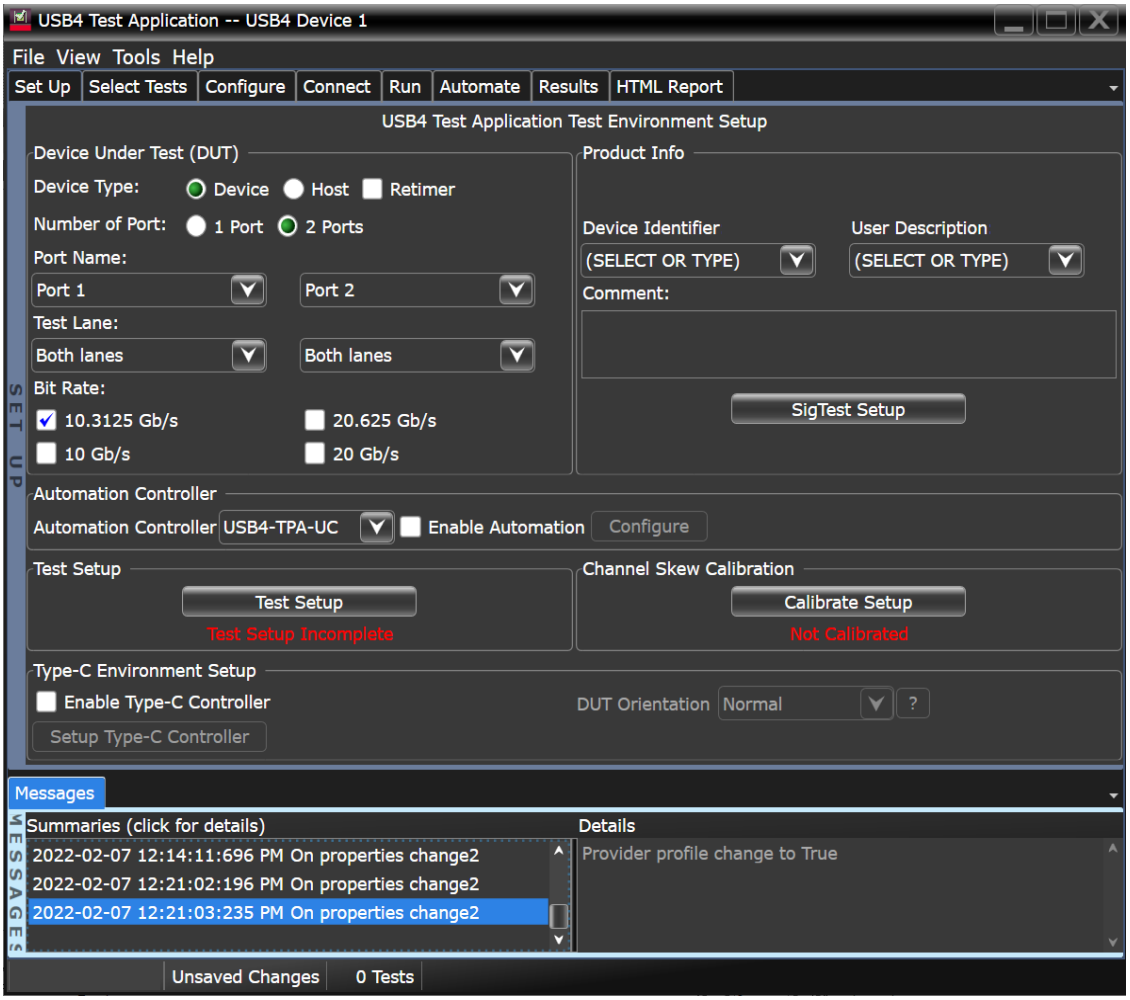


Figure 5 USB4 Test Application default window on 4-Ch Oscilloscope

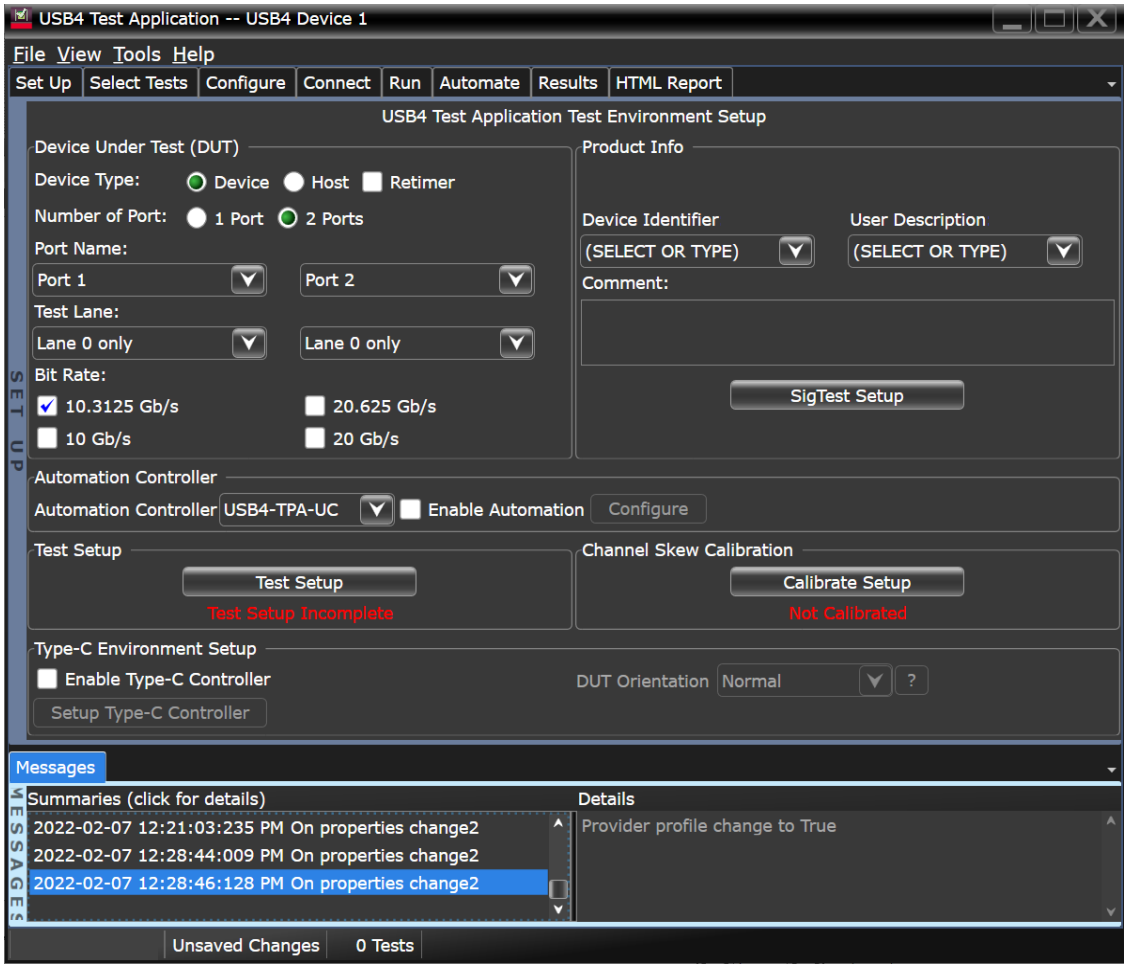


Figure 6 USB4 Test Application default window on 2-Ch Oscilloscope

To understand the functionality of the various features in the user interface of the Test Application, refer to the *Keysight D9040USBC USB4 Compliance Test Application Online Help* available in the Help menu.

The task flow pane and the tabs in the main pane show the steps you take in running the automated tests:

Set Up	Lets you identify and set up the test environment, including information about the device under test. The Test App includes relevant information in the final HTML report.
Select Tests	Lets you select the tests you want to run. The tests are organized hierarchically so you can select all tests in a group. After tests are run, status indicators show which tests have passed, failed, or not been run, and there are indicators for the test groups.
Configure	Lets you configure test parameters (for example, channels used in test, voltage levels, etc.).
Connect	Shows you how to connect the oscilloscope to the device under test for the tests that are to be run.
Run	Starts the automated tests. If the connections to the device under test need to be changed while multiple tests are running, the tests pause, show you how to change the connection, and wait for you to confirm that the connections have been changed before continuing.
Automate	Lets you construct scripts of commands that drive execution of the application.
Results	Contains more detailed information about the tests that have been run. You can change the thresholds at which marginal or critical warnings appear.
HTML Report	Shows a compliance test report that can be printed.

NOTE

In the **Configure** tab, the values for all such configuration parameters that are oscilloscope-dependent, will correspond to the oscilloscope model (DSOs or UXRs), where you are running the Test Application.

Setting up the USB4 Test Application

In order to run the electrical compliance tests on a USB DUT operating at a bit rate of either 10.3125 GB/s, 20.625 GB/s, 10 GB/s. 20 GB/s or all, you must set up the USB4 Test Application to be able to view and select the required tests.

1 Start the USB4 Test Application. See "Starting the USB4 Test Application" on page 45.

2 Under the **Set Up** tab, select the following options, as shown in Figure 7.

a **Device Type:** – Select DUT Type as either **Device** (default) or **Host**.

b **Number of Port:** – Select **1 Port** (default) or **2 Ports**.

c **Port Name:** –This drop-down field allows you to select a port name or even type a custom name for the ports being used for testing. Default values are **Port 1** and **Port 2**.

d **Test Lane:** – The drop-down options, when the Test App is launched on a 4-Channel Oscilloscope, are different from that on a 2-Channel Oscilloscope.

- On a 4-Channel Oscilloscope–From the drop-down options, select either **Both Lanes** (default), **Lane 0 only** or **Lane 1 only**; depending on the number of lanes being used for testing.
- On a 2-Channel Oscilloscope–From the drop-down options, select either **Lane 0 only** or **Lane 1 only**; depending on the number of lanes being used for testing.

e **Bit Rate** – Select either one or more bit-rates to indicate the signal speed on the DUT.

f **Product Info** – Helps you in proper identification of the DUT on HTML reports. This option is particularly useful when running compliance tests on multiple DUTs.

- **Device Identifier:** – Type an appropriate name/identifier for the DUT, which is being tested. The entries are saved such that you may select the values again later, if required.
- **User Description:** – Type an appropriate description for the DUT, which is being tested. The entries are saved such that you may select the values again later, if required.
- **Comment:** – Type appropriate comments, if required.

g **USB Automation Controller** – Select **Enable Automation** check box, then select the required **Automation Controller** from the drop down box. Supported automation controllers are: **USB4-TPA-UC** (Wilder USB4 microcontroller), **TBT-TPA-UHG2** (Wilder Thunderbolt microcontroller), and **TCPIP**.

h **USB Type-C Test Controller** – Select **Enable Type-C Controller** check box, then click the **Setup Type-C Controller** button to configure the **N7018A Type C Test Controller**. Please note, N7018A can only be used with the Wilder Thunderbolt microcontroller.

NOTE

- When testing USB4: Please use the "Wilder USB4 controller + Wilder fixture".
- When testing TBT3: Please use either the "Wilder TBT3 controller + Wilder fixtures" or "the Wilder TBT3 controller + N7018A + N7015A".

For more information about using the **USB Automation Controller** and **USB Type-C Test Controller** features, refer to the *Keysight D9040USBC USB4 Compliance Test Application Online Help*.

i **Test Setup**– Click the **Test Setup** button to set up the following Calibration prerequisites:

- **Preset Calibration** – Required to run the Transmitter Preset Calibration tests.
- **Power Profile** – Appears only when the **Enable Type-C Controller** is selected. Defines the power supply and demand requirements of a USB DUT with Type-C implementation, which may be connected either as a provider or a consumer.

- **Fixture and Cable De-Embed**— Define whether to de-embed a fixture or a cable for all the tests.

j **Channel Skew Calibration** — Click the **Calibrate Setup** button to perform **Channel Skew Calibration** before running the tests. Please perform channel skew calibration on the exact oscilloscope channels where the DUT is connected.

See "Calibration Setup for Compliance Tests" on page 56 for more information on these Calibration options.

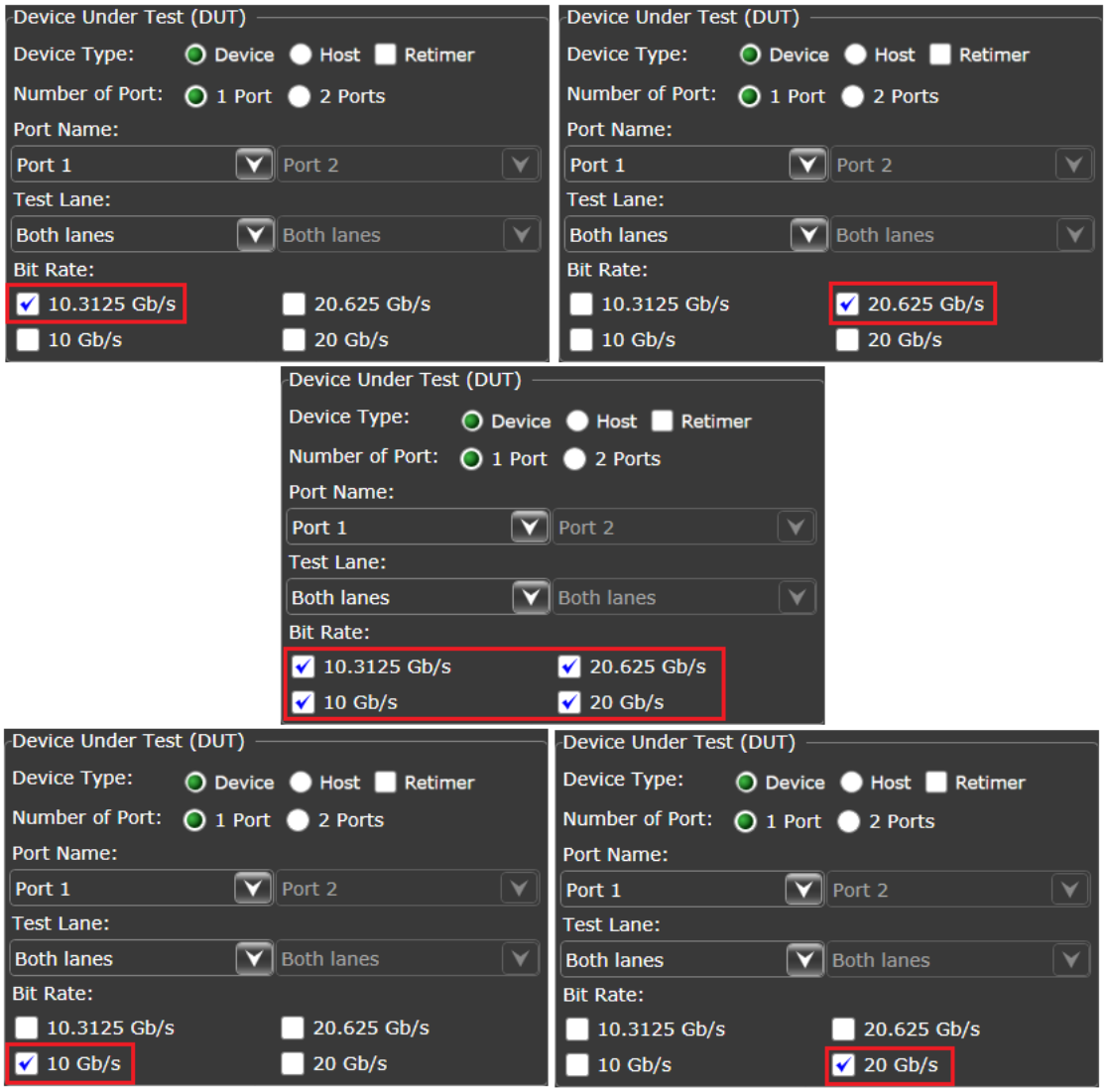


Figure 7 Set Up options for DUT Type "Device" on a 4-Channel Oscilloscope

3 Based on your choices under the **Set Up** tab, the **Select Tests** tab filters tests into test groups corresponding to one or more selected bit-rates and the selected option for device type, port and lane.

For example, Figure 8 shows how test groups are filtered when you select **Device Type:** as **Device**, **Number of Port** as **2 Ports** and **Test Lane:** as **Both lanes** along with selecting all bit rates. Similarly, Figure 9 shows how test groups are filtered when only one bit-rate is selected along with setting

Device Type: as **Host**, **Number of Port** as **1 Port** and **Test Lane:** as **Lane 0 only**. Select the tests that you want to run using the USB4 Test Application. Refer to the *Keysight D9040USBC USB4 Compliance Test Application Online Help* to know more about how to select tests.

NOTE

The **Test Lane** drop-down options in the **Set Up** tab, when the Test App is launched on a 4-Channel Oscilloscope, are different from that on a 2-Channel Oscilloscope. Therefore, on the latter instrument, only **Lane 0 only** or **Lane 1 only** options appear, as otherwise shown in Figure 8.

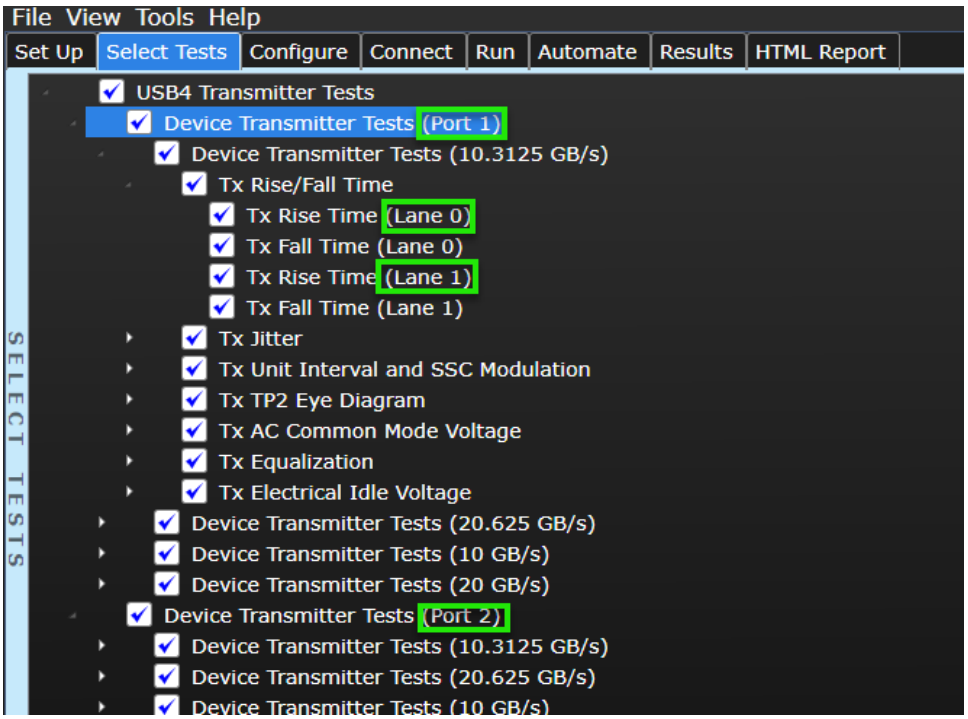


Figure 8 Selecting Transmitter Tests for all bit rates

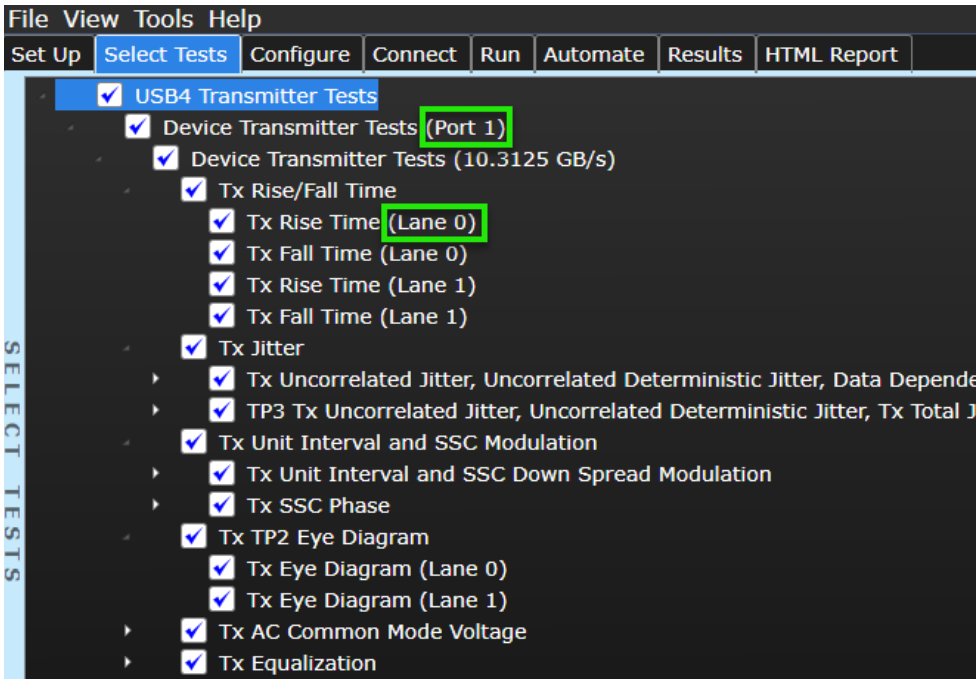


Figure 9 Select Transmitter Tests for a single bit rate

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

4 Under the **Configure** tab, you may modify the values for various configurable options associated with the compliance tests. By default, the USB4 Test Application sets the values of these options to the optimum value according to the standard specifications.

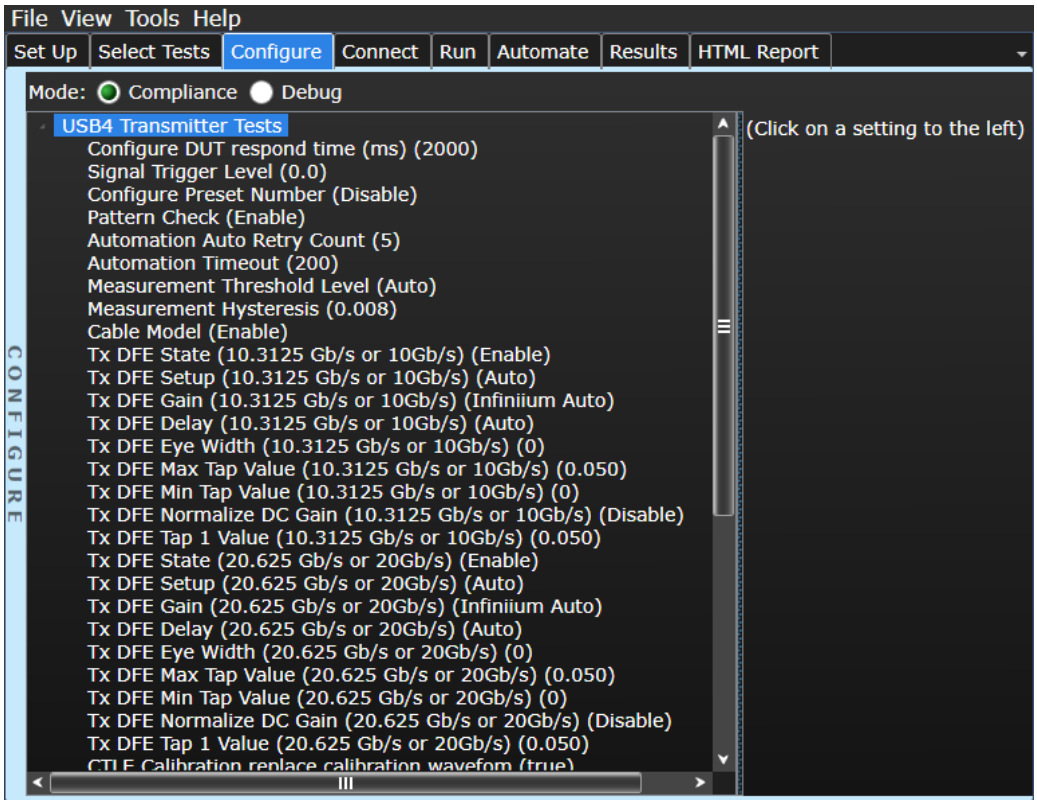


Figure 10 Configure options for USB4 Tests

5 Under the **Connect** tab, the USB4 Test Application displays a Connection Diagram along with a list of instructions. Figure 11 and Figure 12 show the connection diagrams for a 2-Lane set up and for a 1-Lane set up, respectively, on a 4-Channel Oscilloscope, whereas Figure 13 shows the connection diagram for the “Lane 0 Only” set up on a 2-Channel Oscilloscope. If you have already set up a physical connection, you may verify else connect the DUT with the Oscilloscope as shown under this tab. Note that during some test runs, the application may prompt you for a change in physical connection/setup.

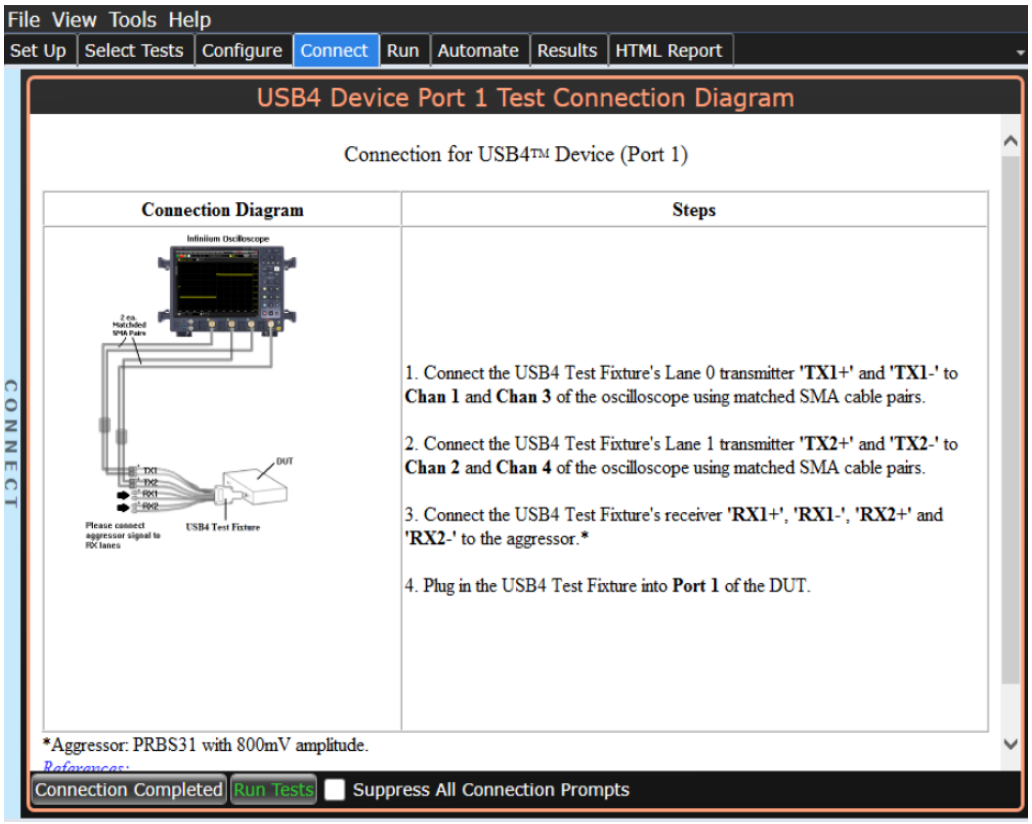


Figure 11 Connection Diagram and Instructions for a 2-Lane test set up on a 4-Ch Oscilloscope

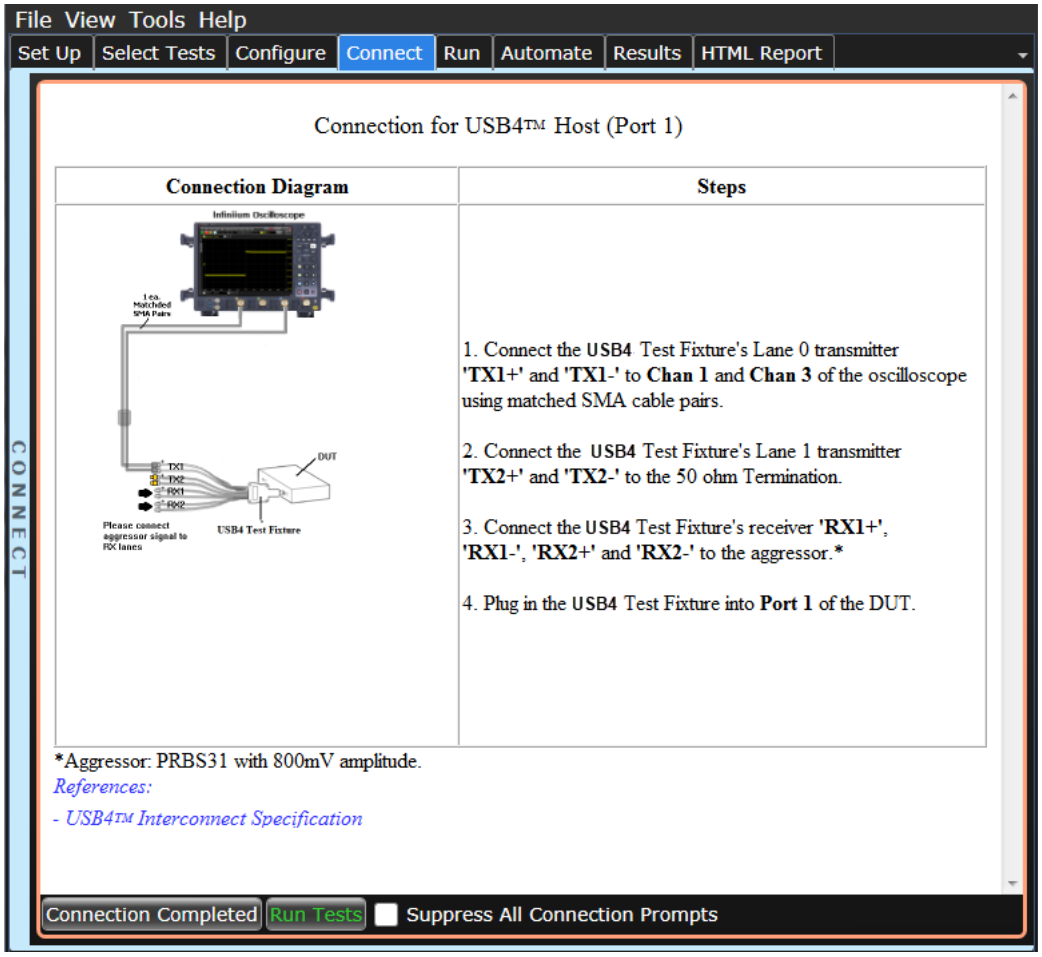


Figure 12 Connection Diagram and Instructions for a 1-Lane test set up on a 4-Ch Oscilloscope

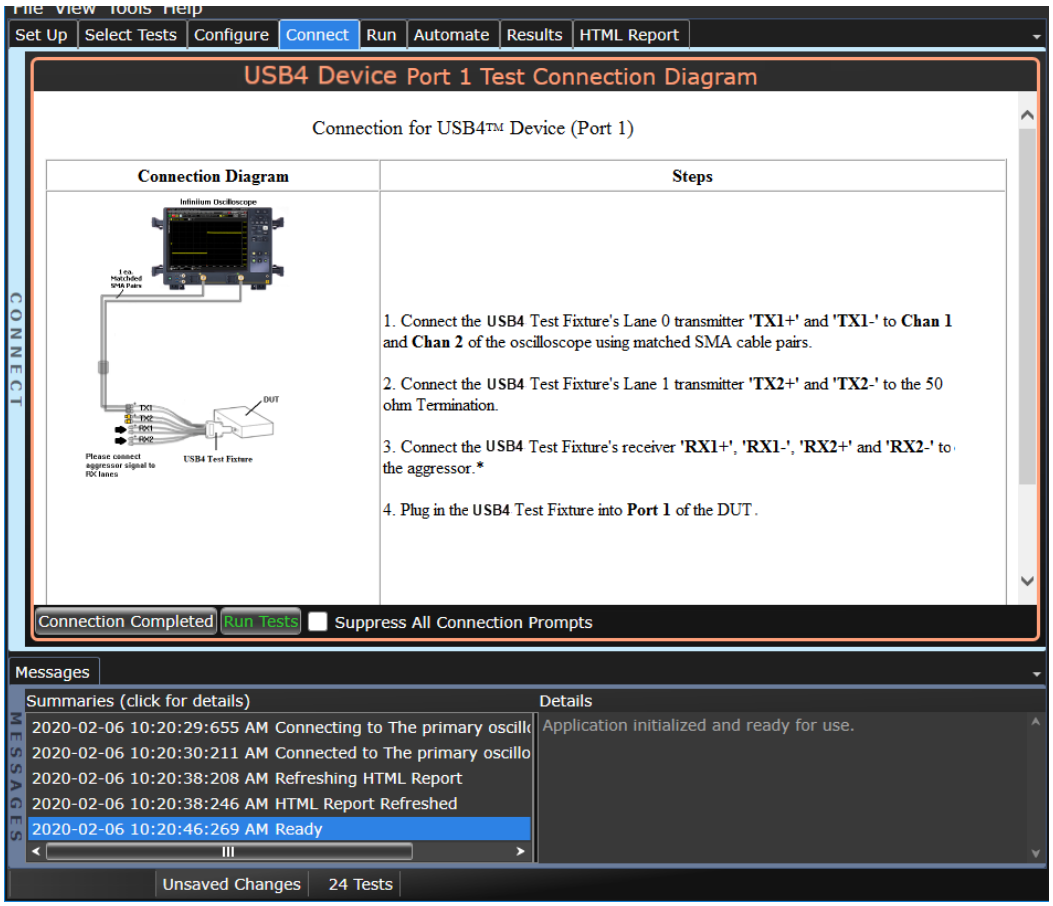


Figure 13 Connection Diagram and Instructions for “Lane 0 Only” on 2-Channel Oscilloscope

6 Once you have performed steps 1 to 5, you are ready to run compliance tests on the USB DUT. Additionally, you may configure/modify the run settings, automate options in the Test Application, view, export and print the test results and the HTML reports generated by the Test Application. Refer to the *Keysight D9040USBC USB4 Compliance Test Application Online Help* to know more about how to use the Test Application.

Calibration Setup for Compliance Tests

Before running compliance tests on a USB DUT, it is imperative that the testing equipment and its accessories be calibrated. The USB4 Test Application provides the options to run Channel Skew Calibration and configure settings for Preset Calibration.

Channel Skew Calibration

In order to achieve accurate test results and to verify that the Device under test is compliant to the standards, it is necessary to calibrate the oscilloscope channels that are connected via cables to the USB DUT.

Perform the following:

1 In the **Channel Skew Calibration** area of the **Set Up** tab of the USB4 Test Application, click the **Calibrate Setup** button.

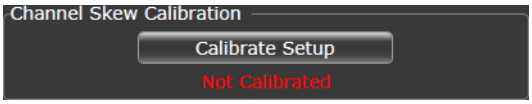


Figure 14 Channel Skew Calibration area under the **Set Up** tab

2 The **Calibration** window appears, where the **Channel Skew Calibration** tab is displayed by default, as shown in Figure 15 for a 4-Channel Oscilloscope and in Figure 16 for a 2-Channel Oscilloscope.

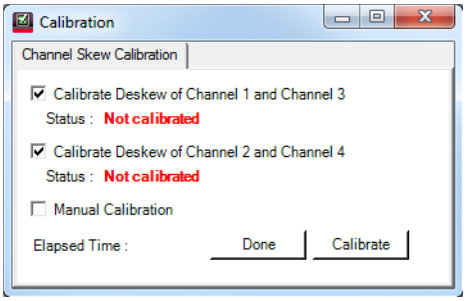


Figure 15 Options for Channel Skew Calibration on a 4-Channel Oscilloscope

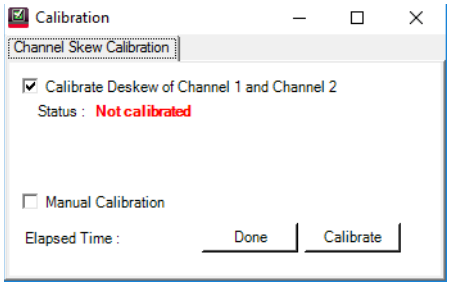


Figure 16 Options for Channel Skew Calibration on a 2-Channel Oscilloscope

Under the **Channel Skew Calibration** tab, the USB4 Test Application displays the status of the oscilloscope channels that have been calibrated for de-skew. As shown in the images above, the options are checked by default and the status of each of these options is **Not Calibrated**. You may also select the **Manual Calibration** check box to perform Channel Skew Calibration later.

To start Calibration of the selected Oscilloscope channel pairs, click the **Calibrate** button. The **Test Instruction for USB4 Compliance** window appears.

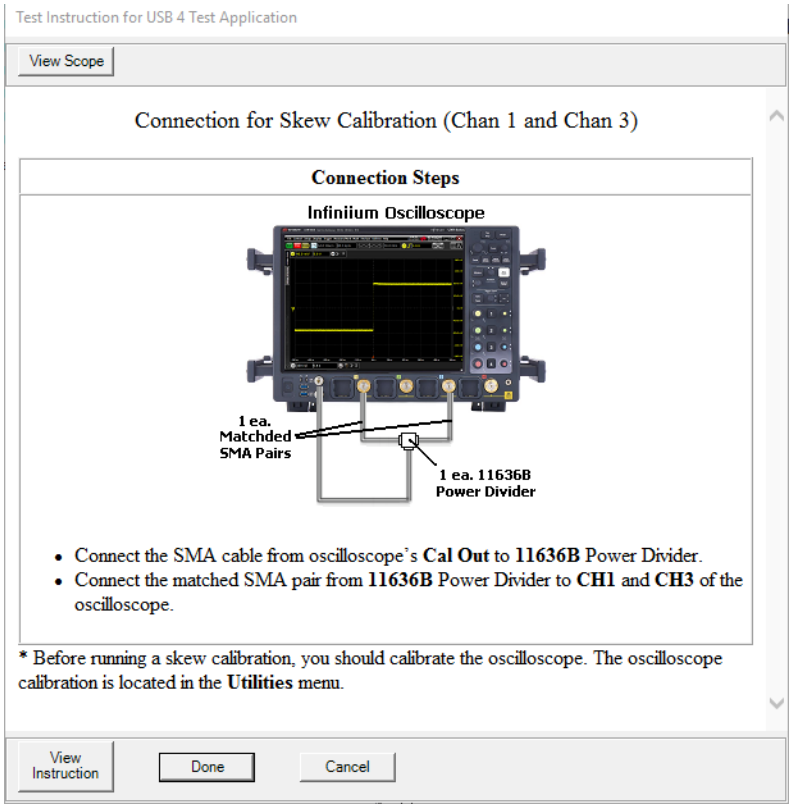


Figure 17 Instructions for Channel Skew Calibration for the selected Channels on a 4-Ch Oscilloscope

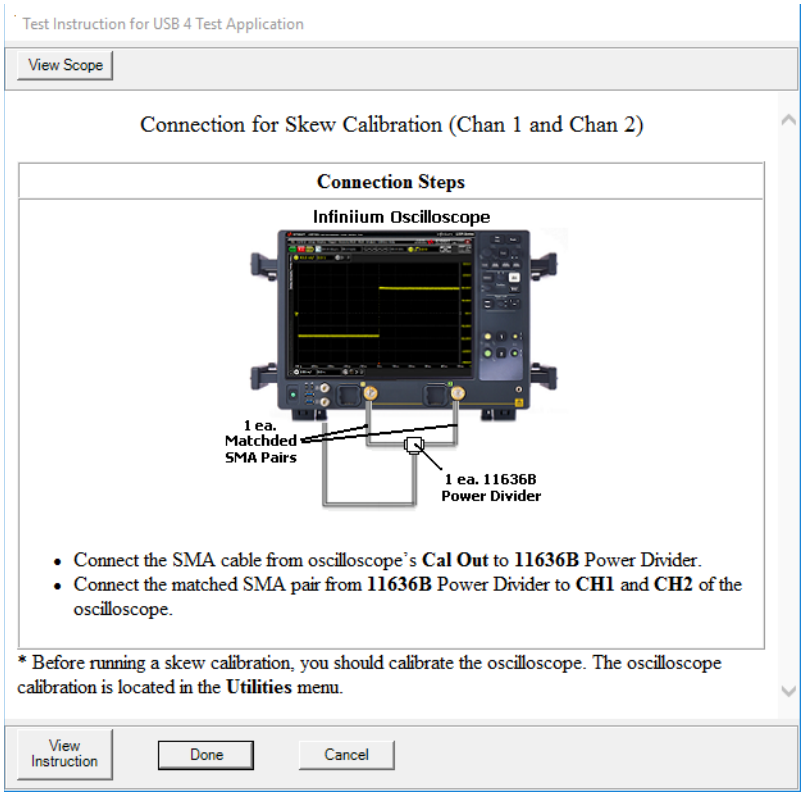


Figure 18 Instructions for Channel Skew Calibration for the selected Channels on a 2-Ch Oscilloscope

The **Test Instruction for USB4 Compliance** window provides instructions and connection diagram required to be set up to perform Channel Skew Calibration.Note that before you start performing Channel Skew Calibration, the oscilloscope must have been calibrated.

On the **Test Instruction for USB4 Compliance** window,

1 Click the **View Scope** button to minimize this window and to see the oscilloscope screen for the waveform and to use the Infiniium controls to perform oscilloscope calibration (if it has not been done yet).

2 Click the **View Instruction** button to maximize the window to view the instructions and the connection diagram again.

3 Once you have set up the physical connection for Channel Skew Calibration for the respective channels, click **Done** to begin Calibration.You may click **Cancel** at any point to simply return to the **Calibration** window.

When you click **Done**, the **Calibration** window displays again with the updated Status along with the time elapsed during this process, as shown in Figure 19 and Figure 20.

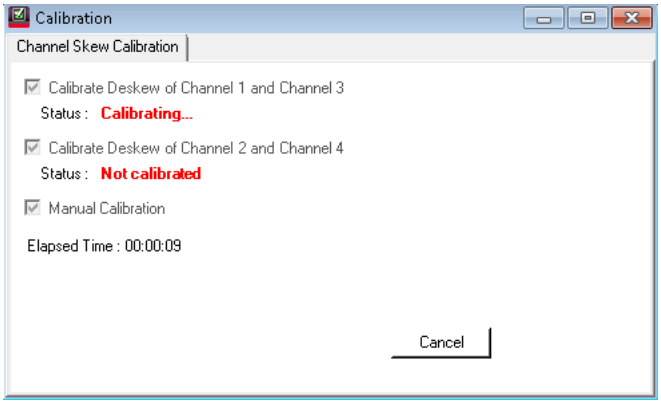


Figure 19 Changes in Calibration status on a 4-Channel Oscilloscope

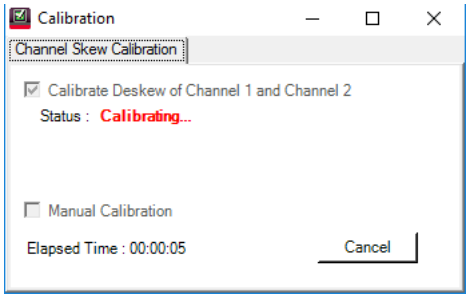


Figure 20 Changes in Calibration status on a 2-Channel Oscilloscope

Once the Calibration process is successfully completed, the status changes to **Calibrated**. You may click **Cancel** to stop the process of Channel Skew Calibration at any time.

4 After the Channel Skew Calibration is complete, click the **Done** button to return to the USB4 Test Application Test Environment Setup.

Preset Calibration

The **Preset Calibration** tab allows you to select the preset number, which has been set on the USB DUT, to be used in the USB4 Test Application. You may also perform the preset sweep to find the optimum preset.

Perform the following:

1 In the **Test Setup** area of the **Set Up** tab of the USB4 Test Application, click the **Test Setup** button.

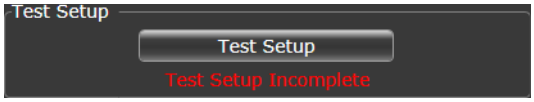


Figure 21 Test Setup area under the **Set Up** tab

2 The **Test Setup** window appears, where the **Preset Calibration** tab is displayed by default, as shown in Figure 22 for a 4-Channel Oscilloscope and Figure 23 for a 2-Channel Oscilloscope.

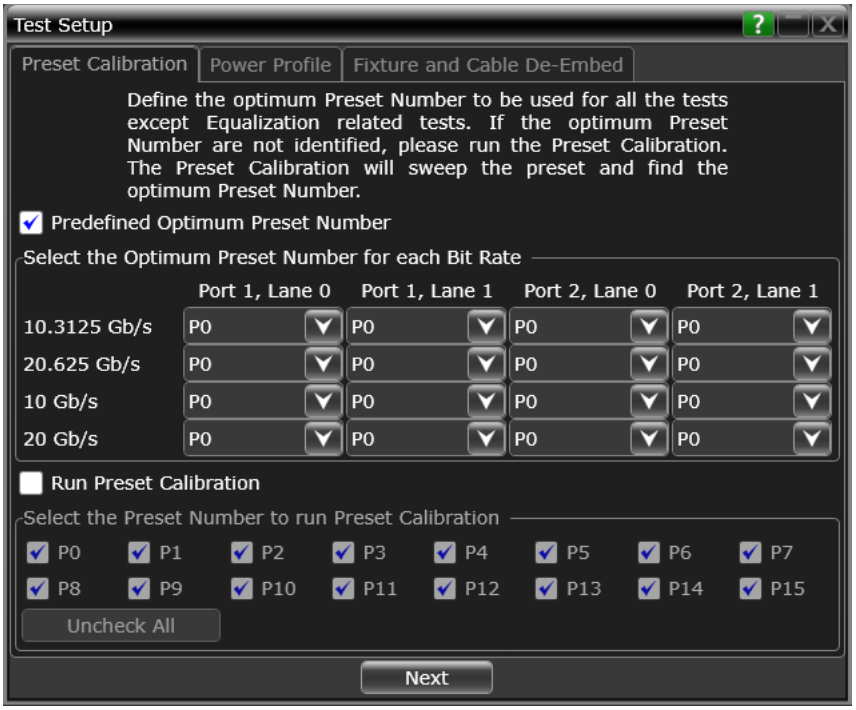


Figure 22 Default view of the Preset Calibration tab on a 4-Channel Oscilloscope

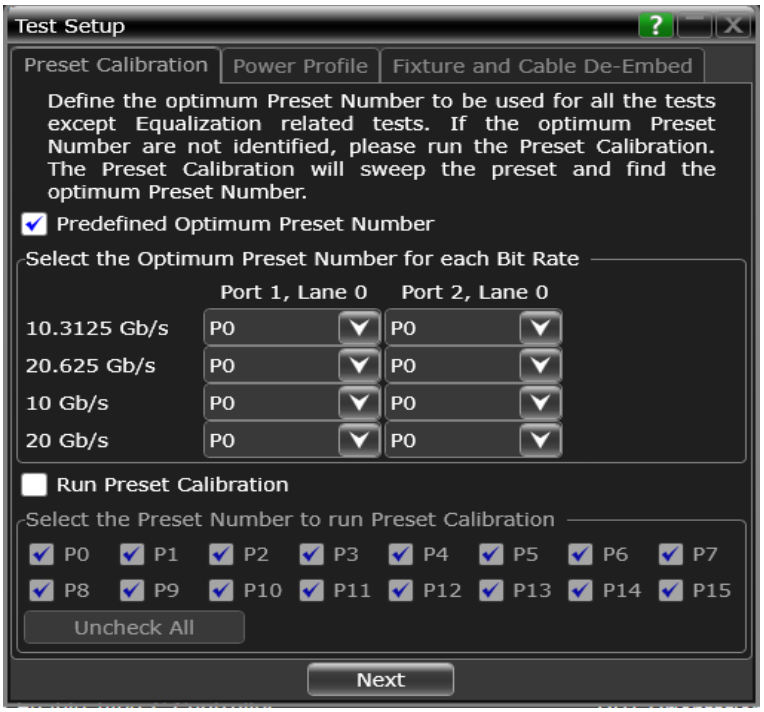


Figure 23 Default view of the Preset Calibration tab on a 2-Channel Oscilloscope

Under the **Preset Calibration** tab,

1 By default, the **Predefined Optimum Preset Number** check-box is selected and the default Preset Number for the selected bit rates is set to **P0**.

2 From the **Select the Optimum Preset Number for each Bit Rate** area, select a preset number from the drop-down options corresponding to each bit-rate and port-lane combination.

3 Select the **Run Preset Calibration** check-box only if you wish to run Preset Calibration to find the optimum preset value for the DUT. By default, all preset values are selected.

4 In the **Run Preset Calibration**, you may de-select any of the preset numbers to exclude them from preset Calibration.You may use the **Uncheck All** or **Check All** radio buttons to perform this action as well.

NOTE

By default, the test group for **Preset Calibration** for each selected bit-rate is hidden in the **Select Tests** tab when **Predefined Optimum Preset Number** is selected for the respective bit-rates. To view and select the **Preset Calibration** tests in the **Select Tests** tab, select the **Run Preset Calibration** option in the **Test Setup** window of the **Set Up** tab.

5 Click **Next** to move to the next tab.

Power Profile

The **Power Profile** tab allows you to select the voltage and current requirements when the USB DUT with the Type-C implementation is connected for testing.

NOTE **Power Profile** tab will be visible only if in the **Set Up** tab, **Enable Type-C Controller** check box is selected.

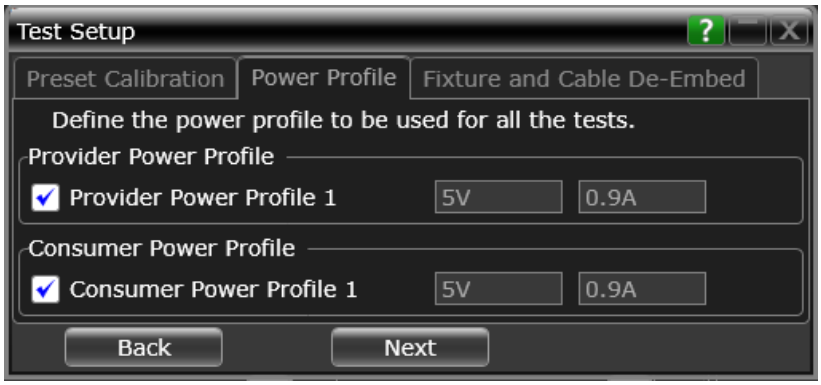


Figure 24 Default view of the Power Profile tab

Under the **Power Profile** tab,

1 Use the check-box to select or de-select one of listed **Provider Power Profile** or **Consumer Power Profile** options.

   If the connected USB4 DUT with Type-C behaves as the source of power supply, it is identified and denoted as Provider Power Profile. If the DUT consumes power, it is identified and denoted as Consumer Power Profile.

2 The number of power profiles displayed varies based on the power profile supported by the DUT, which in turn, is obtained during the DUT Capability Query.

3 Click **Next** to move to the next tab.

Fixture and Cable De-Embed

The **Fixture and Cable De-Embed** tab allows you to define whether to de-embed fixture, or cable, or both for all the tests.

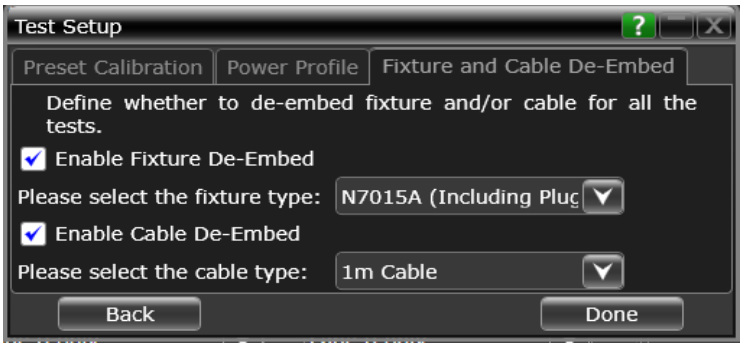


Figure 25 Default view of the Fixture and Cable De-Embed tab

Under the Fixture and Cable De-Embed tab,

1 Select the **Enable Fixture De-Embed** check box to de-embed a fixture. Then, from the drop-down box, **Please select the fixture type**. One of the following three fixture types can be selected:

- **N7015A (Including Plug)**
- **N7015A (Not Including Plug)**
- **Custom** - If custom fixture is selected, an **S-Parameter File** needs to be provided for Lane 0 and Lane 1. Use the **Browse** option to select the system location of the s-parameter file. In case, there are **Different s-parameter files for Lane 0 and Lane 1**, please select two different s-parameter files for the custom fixture.

NOTE

In case of two different s-parameter files, it is important that the file names are different even if the files are at different system locations.

The application identifies the s-parameter file using the file name. S-parameter files with the same name but different system locations will be considered as the same file.

2 Select the **Enable Cable De-Embed** check box to de-embed a cable. Then, from the drop-down box, **Please select the cable type**. One of the following two cable types can be selected:

- **1m Cable**
- **Custom** - If custom cable is selected, an **S-Parameter File** needs to be provided for Lane 0 and Lane 1. Use the **Browse** option to select the system location of the s-parameter file. In case, there are **Different s-parameter files for Lane 0 and Lane 1**, please select two different s-parameter files for the custom cable. Also, please see the note in point 1 for s-parameter file naming.

3 Click **Done** to save any modifications done to the **Fixture and Cable De-Embed** tab, and to return to the USB4 Test Application Test Environment Setup.

4 Host / Device USB4 Transmitter Testing

Architectural Overview / 66
USB4 Electrical Compliance Methodology / 68
Router Assembly Transmitter Compliance / 73

The Keysight D9040USBC USB4 Compliance Test Application USB4 Test Application enables compliance testing of the Host and Device Transmitter systems operating at bit rates of 10.3125 GB/s, 20.625 GB/s, 10 GB/s, or 20 GB/s, based on Universal Serial Bus 4 (USB4™) Specification version 1.0, August 2019.

NOTE

As per the USB4 Specification Version 1.0:

- Gen 2 refers to speeds of 10 Gbps (USB4) and/or 10.3125 Gbps (TBT3-Compatibility Mode).
- Gen 3 refers to speeds of 20 Gbps (USB4) and/or 20.625 Gbps (TBT3-Compatibility Mode).

Architectural Overview

This section presents an overview of Universal Serial Bus 4 (USB4™) architecture and key concepts.

Overview

USB4 is similar to earlier versions of USB in that it is a cable bus supporting data exchange between a host computer and a wide range of simultaneously accessible peripherals. However, USB4 also allows a host computer to set up data exchange between compatible peripherals. The attached peripherals share bandwidth as configured by the host computer. The bus allows peripherals to be attached, configured, used, and detached while the host and other peripherals are in operation.

When configured over a USB Type-C® connector interface, USB4 functionally replaces USB 3.2 while retaining USB 2.0 bus operating in parallel. Enhanced SuperSpeed USB, as defined in USB 3.2, remains the fundamental architecture for USB data transfer on a USB4 Fabric. The difference between USB4 and USB 3.2 is that USB4 is a connection-oriented, tunneling architecture designed to combine multiple protocols onto a single physical interface, so that the total speed and performance of the USB4 Fabric can be dynamically shared. USB4 allows for USB data transfers to operate in parallel with other independent protocols specific to display, load/store and host-to-host interfaces. Additionally, USB4 extends performance beyond the 20 Gbps (Gen 2 x 2) of USB 3.2 to 40 Gbps (Gen 3 x 2) over the same dual -lane, dual-simplex architecture.

The specification introduces the concept of protocol tunneling to USB bus architecture. Besides tunneling Enhanced SuperSpeed USB (USB3), display tunneling based on DisplayPort (DP) protocol and load/store tunneling based on PCI Express (PCIe) are defined. These protocol tunnels operate independently over the USB4 transport and physical layers. Additionally, USB4 allocates packets for bus configuration and management, and packets can be allocated specifically for host-to-host data connections.

USB4 System Description

Figure 26 illustrates the dual bus architecture of USB 3.2 as augmented by USB4. As architectured, backward compatibility is supported with minimum interoperability starting at USB 2.0, working up through USB 3.2, and finally up to USB4 based on the highest common bus level supported across the interconnected components. Protocol tunnels are interfaced via Protocol Adapters specific to each protocol. For USB and PCIe protocols, native USB hubs and PCIe switches are required to handle protocol -related packet routing and buffering. For display tunneling, no intermediate DP-specific logic is required with display tunnels being established as an end-to-end link. Time synchronization across a USB4 Fabric uses distributed time management units (TMUs) associated with each Router.

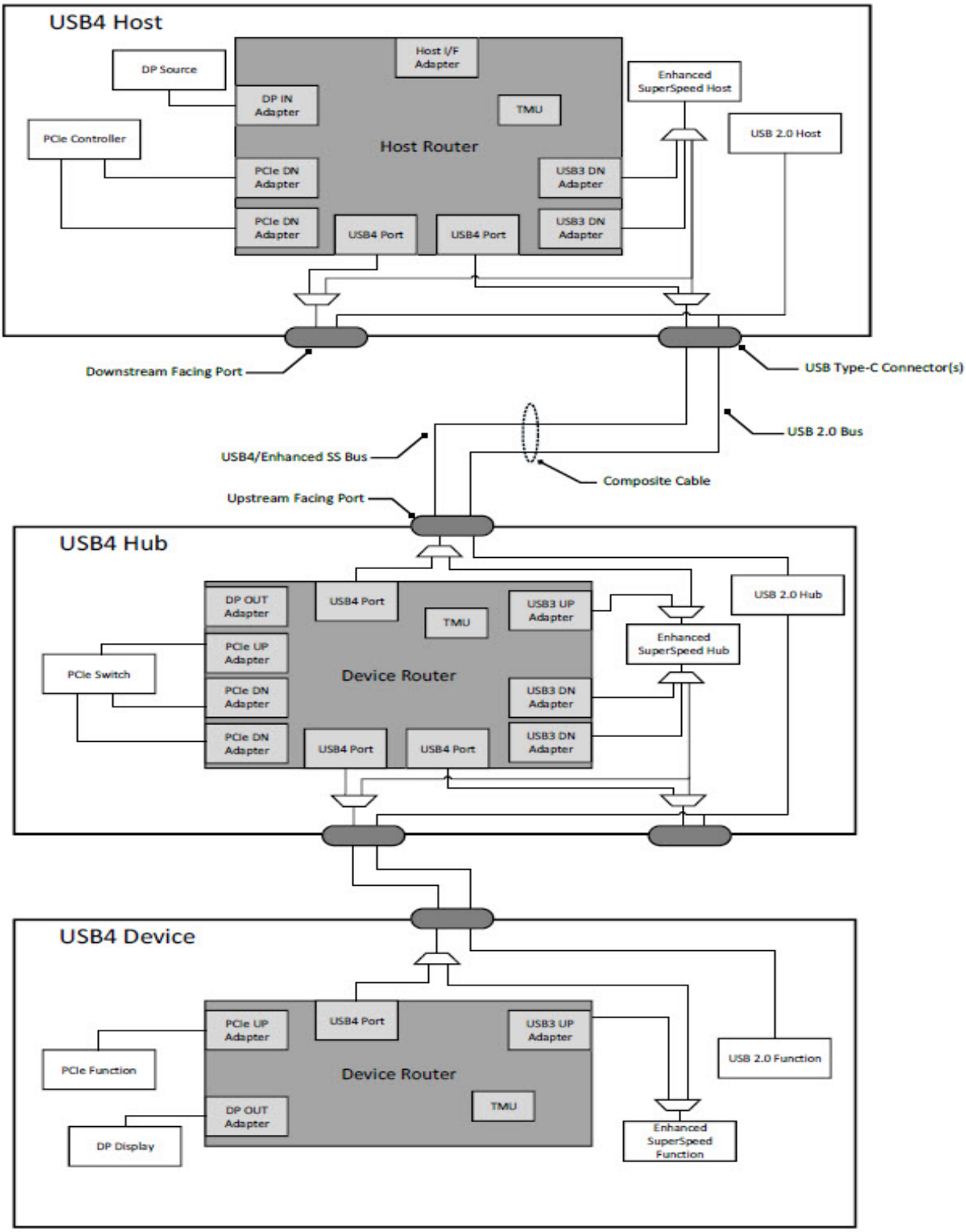


Figure 26 USB4/USB3.2 Dual Bus System Architecture

USB4 Electrical Compliance Methodology

System Compliance Test Point Definitions

All measurements shall be referenced to the electrical compliance test points in Table 2. Calibration shall be applied in cases where direct measurement is not feasible.

Table 2 Electrical Compliance Test Points

Test Point	Description	Comments
TP1	Transmitter IC output	Not used for electrical testing.
TP2	Transmitter port connector output	Measured at the plug side of the connector.
TP3	Receiver port connector output	Measured at the receptacle side of the connector. All the measurements at this point shall be done while applying reference equalization function.
TP3'	Receiver port connector input	Measured at the plug side of the connector.
TP4	Receiver IC input	Not used for electrical testing.

.

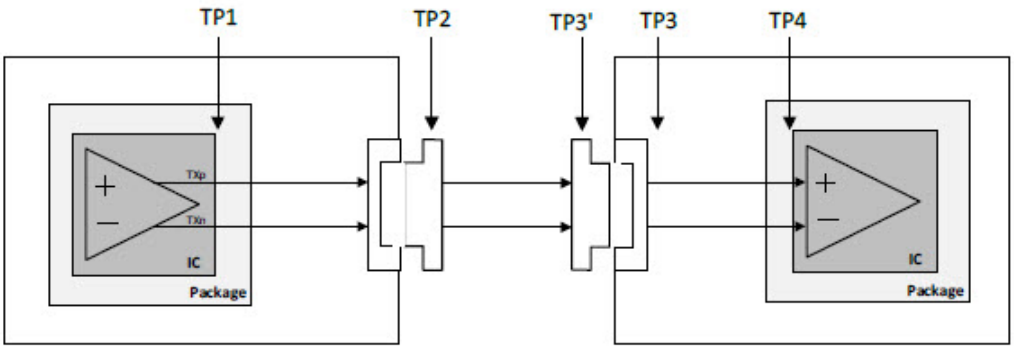


Figure 27 Compliance Points Definition

Reference Clock-and-Data-Recovery (CDR) Function

All jitter and eye diagram measurements shall be performed while applying a reference clock - and-data-recovery (CDR) function. The reference CDR is modeled by a 2nd order PLL response (type II), which derives the following jitter transfer function, described in Laplace domain:

$$H_{jitter}(s) = \frac{s^2}{s^2 + 2 \cdot \zeta \cdot \omega_n \cdot s + \omega_n^2}$$

where

s is the frequency in Laplace domain
ζ is the damping factor
ω_n is the natural frequency of the system

The damping factor and natural frequency used for compliance testing shall be 0.94 and 2.2E7 rad/sec respectively, forming High-Pass-Filter (HPF) mask with 3 dB bandwidth at 5 MHz.

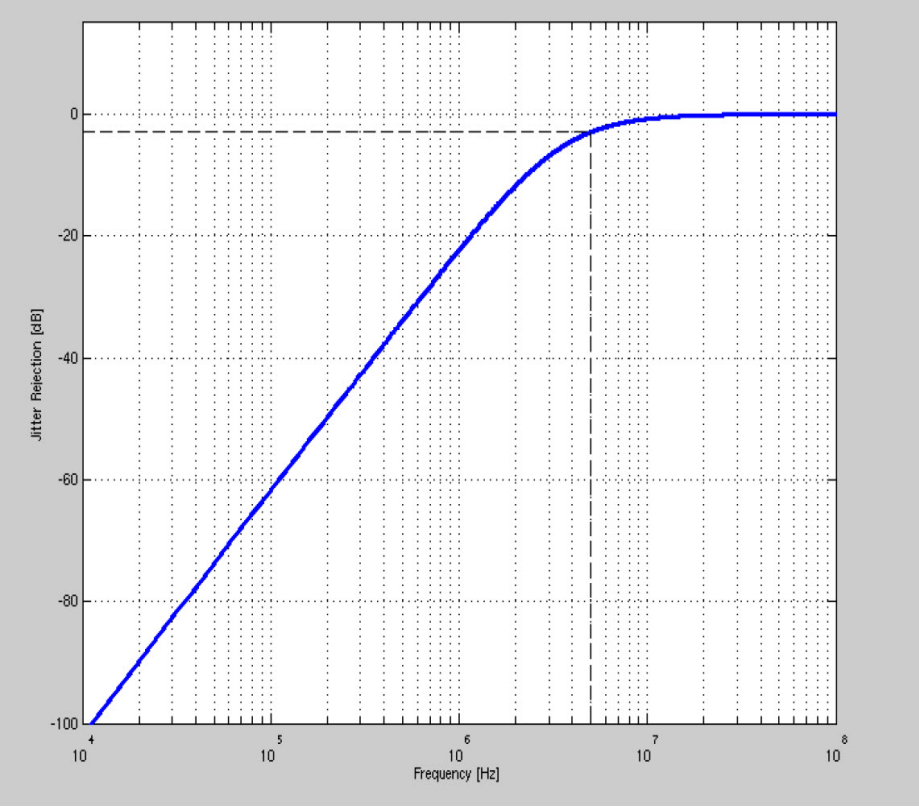


Figure 28 Jitter Transfer Function

Reference Equalization Function

All the measurements at TP3 compliance point shall be performed while applying a reference receiver equalization function. The reference receiver equalization function is comprised of parametric Continuous-Time-Linear-Equalizer (CTLE) and Decision-Feedback-Equalizer (DFE), as described in following sections.

A measurement that is referenced to TP3 shall use equalization parameters that optimize the calculated eye-diagram.

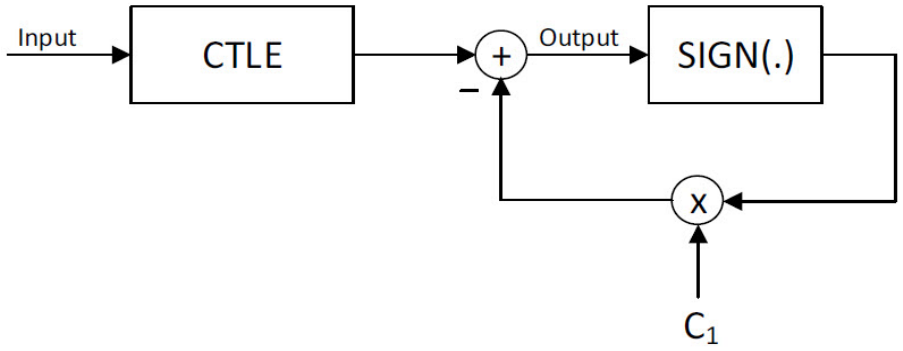


Figure 29 Reference Receiver Equalization

Reference CTLE

The following equation describes the frequency response for the USB4 reference CTLE that shall be used for compliance testing:

$$H(s) = 1.41 \cdot \omega_{p2} \cdot \frac{s + \frac{A_{DC}}{1.41} \cdot \omega_{p1}}{(s + \omega_{p1}) \cdot (s + \omega_{p2})}$$

where

A_{DC} is the DC gain
s is the frequency in Laplace domain

$$\omega_{p1} = \begin{cases} 2 \cdot \pi \cdot 1.5e^9 \frac{rad}{sec} & Gen\ 2 \\ 2 \cdot \pi \cdot 5e^9 \frac{rad}{sec} & Gen\ 3 \end{cases}$$

$$\omega_{p2} = \begin{cases} 2 \cdot \pi \cdot 5e^9 \frac{rad}{sec} & Gen\ 2 \\ 2 \cdot \pi \cdot 10e^9 \frac{rad}{sec} & Gen\ 3 \end{cases}$$

Ten different CTLE configurations shall be applied such that A_{DC} is one of $\left\{10^{\frac{-x}{20}} : x = 0, 1, \ldots, 9\ [dB]\right\}$.

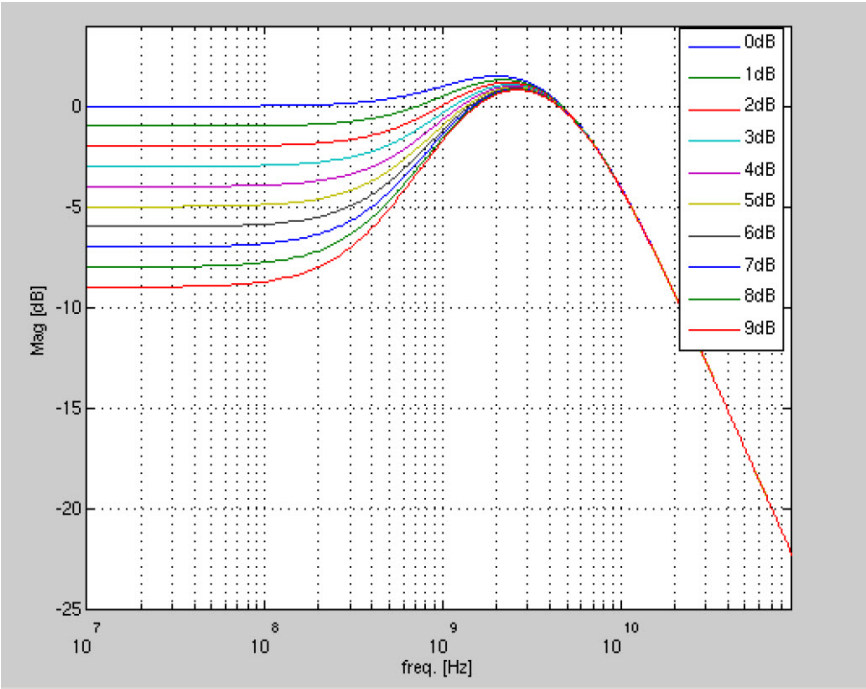


Figure 30 Frequency Response of Gen 2 Reference CTLE

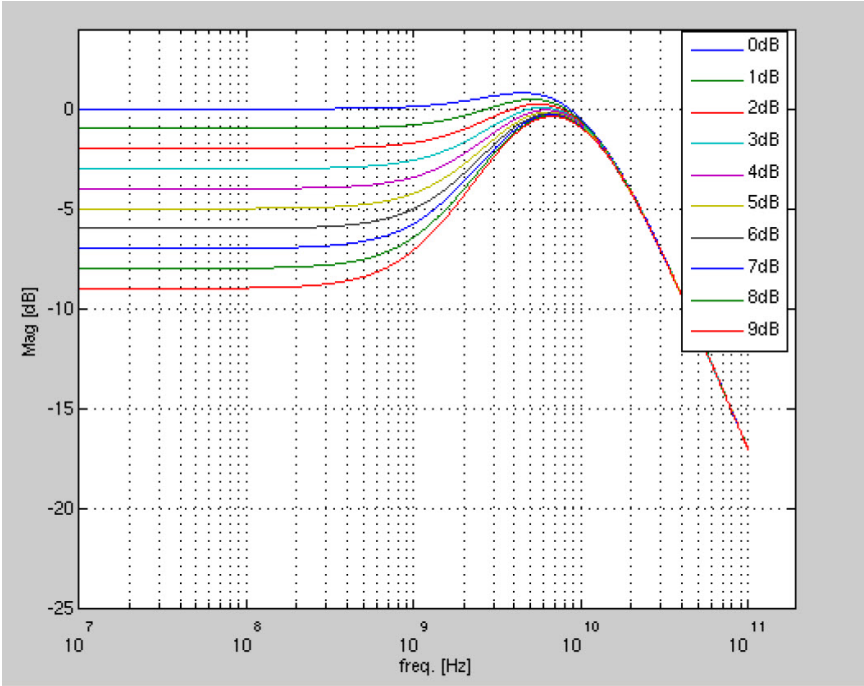


Figure 31 Frequency Response of Gen 3 Reference CTLE

Reference DFE

A 1-tap feedback filter is defined as part of the reference receiver equalizer used in the compliance testing. The DFE formula is described in the following equation:

$$Y_n = X_n - C_1 * \text{sign}(Y_{n-1})$$

where:

Y_n is the DFE output at time instant n
X_n is the DFE input (incoming signal after applying CTLE) at time instant n
C_1 is the DFE coefficient, which shall be limited to a range of 0 mV to 50 mV

Router Assembly Transmitter Compliance

Transmitter compliance testing for a Router Assembly is defined at two measurement points:

- The output of a compliance plug fixture at the TP2 reference point.
- The output of a compliance receptacle fixture at the TP3 reference point.

Compliance Plugs and Compliance Receptacles are defined in Section 3.3.6.1 (Compliance Plug Test Board) and Section 3.3.6.2 (Compliance Receptacle Test Board), respectively, of the USB4 Specification Version 1.0.

Unless otherwise specified, a transmitter shall drive PRBS31 pattern during compliance testing. All tests shall be performed with Spread-Spectrum-Clocking (SSC) enabled and while all neighboring transceivers are active.

Transmitter Specifications Applied for All Speeds

Table 3 defines the transmitter parameters that shall apply for both Gen 2 and Gen 3 modes of operation.

Table 3 Transmitter Specifications Applied for All Speeds (at TP2)

Symbol	Description	Min	Max	Units	Conditions
RL_DIFF	Differential Return Loss, 0.05-12GHz	---	See section: "Transmitter Differential Return Loss"	dB	
RL_COMM	Common Mode Return Loss, 0.05 – 12GHz	---	See section: "Transmitter Common Mode Return Loss"	dB	
TX_EQ	Transmitter Equalization Setting	---	See section: "Transmit Equalization"		
SSC_DOWN_SPREAD_RANGE	Dynamic range of SSC down-spreading during steady-state	0.4	0.5	%	See Note 3, Note 4, and Figure 33
SSC_DOWN_SPREAD_RATE	SSC down-spreading modulation rate during steady-state	30	33	kHz	See Note 4 and Figure 33
SSC_PHASE_DEVIATION	Phase jitter associated with the SSC modulation during steady-state	2.5	2.2	ns pp	See Note 1, Note 4, and Figure 33
SSC_SLEW_RATE	SSC frequency slew rate (df/dt) during steadystate	---	1250	ppm/µs	See Note 2, Note 4, and Figure 33
TX_FREQ_VARIATIONS_TRAINING	TX frequency variation during Link training, before obtaining steadystate	---	See section: "Transmitter Frequency Variations during Link Training"	ppm	See Note 4
LANE_TO_LANE_SKEW	Skew between dual transmit signals of the same USB4 Port	---	26	ns	See Note 5
RISE_FALL_TIME	TX rise/fall time measured between 20-80% levels	10	---	ps	Test pattern shall be SQ128 (see Table 8-56 of the USB4 Specification Version 1.0).
V_ELEC_IDLE	Peak voltage during transmit electrical idle (one-sided voltage opening of the differential signal)	---	20	mV	See Note 6.
V_TX_DC_AC_CONN	Instantaneous DC+AC voltages at the connector side of the AC coupling capacitors	-0.5 (min1) -0.3 (min2)	1.0	V	See Note 7.

Notes for Table 3**:**

1 SSC phase deviation shall be extracted from the transmitted signal . During this test, the transmitter shall be configured to send PRBS31 pattern. The SSC phase deviation shall be extracted from the signal phase after applying a 2nd order low-pass filter with 3 dB point at 5 MHz.

2 The SSC slew rate shall be extracted from the transmitted signal over measurement intervals of 0.5 µs. The SSC slew-rate shall be extracted from the signal phase after applying a 2nd order low-pass filter with dB point at 5 MHz.

3 SSC_DOWN_SPREAD_RANGE specifies the required SSC modulation depth, represented by the difference of the maximum and minimum modulated frequencies, referenced to the Link speed.

4 Steady-state clocking is applied from the point that SLOS training pattern is sent by the transmitter.

5 Total Lane-to-Lane skew measured at TP2 including the skew introduced by the physical media, by the Router IC TX, and by up to 2 re-timers placed on the board. Informative Lane-to-Lane skew budget: Router IC TX pins: 8 ns, each Re-timer input-to-output: 8 ns, physical media mismatches: 2ns.

6 V_ELEC_IDLE shall be extracted after applying first order low-pass filter with 3 dB point at 1.25 GHz.

7 The absolute single-ended voltage seen by the receiver. This requirement applies to all link states and during power-on, and power-off. (min1, max) is measured with a 200 kΩ receiver load, and (min2, max) is measured with a 50 Ω receiver load. The ground offset between a DFP and UFP does not contribute to V_TX_DC_AC_CONN.

Transmitter Frequency Variations during Link Training

Background (Informative)

A USB4 link can include up to 6 Re-timers, which forward data from one end of the Link to the other end. During Link training, the transmitters at both ends of the Link send SLOS pattern. The SLOS pattern is clocked with SSC down spreading as specified in Table 3. Re-timer transmitters on the Link are all enabled in parallel. Initially, the Re-timer transmitters do not forward the incoming data and just send CL_WAKE1.X ordered sets clocked at a local constant frequency (without SSC modulation). In the later stages of the Link training, the Re-timer transmitters sequentially switch to forwarding the incoming data at the incoming frequency. As soon as all of the Re-timer transmitters complete the switching process, steady state is obtained and SLOS pattern clocked with SSC is forwarded from one end of the Link to the other. If a Link does not include any Re-timers, the transmitter frequency modulation is at its steady state from the beginning of the Link training period, as clock switching does not take place.

Transmitter Specifications Applied to All Speeds

Table 4 specifies the limits on the transmitter frequency variation during Link training of a Router Assembly that includes one or more Re-timers:

Table 4 Transmitter Frequency Variation Limits During Link Training Before Obtaining Steady-State

Symbol	Description	Min	Max	Units	Conditions
INIT_FREQ_VARIATION	Initial non-modulated transmit frequency applied while sending CL_WAKE1.x pattern	-300	300	ppm	See Note 1
DELTA_FREQ_200ns	Frequency variation during Link training over 200ns measurement windows	---	1400	ppm	See Note 1
DELTA_FREQ_1000ns	Frequency variation during Link training over 1is measurement windows	---	2200	ppm	See Note 1

Notes for Table 4:

1 Measurement shall be performed over the transmitted signal. The signal phase shall be extracted while applying a 2^{nd} order low-pass filter with 3 dB point at 5 MHz.

As shown in the example depicted in Figure 32, the initial transmit frequency of a Router Assembly employing Re-timers is not modulated. The transmit frequency variation following the clock-switching event shall be measured over time intervals of 200 ns and 1 µs.

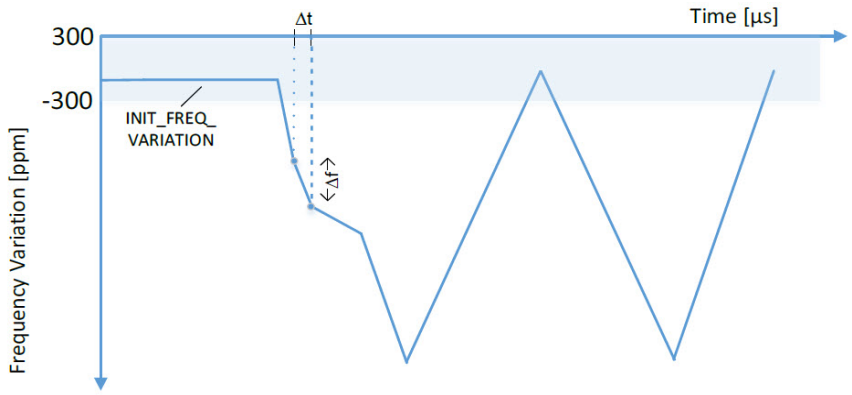


Figure 32 Example Transmitter Frequency Variation During Training

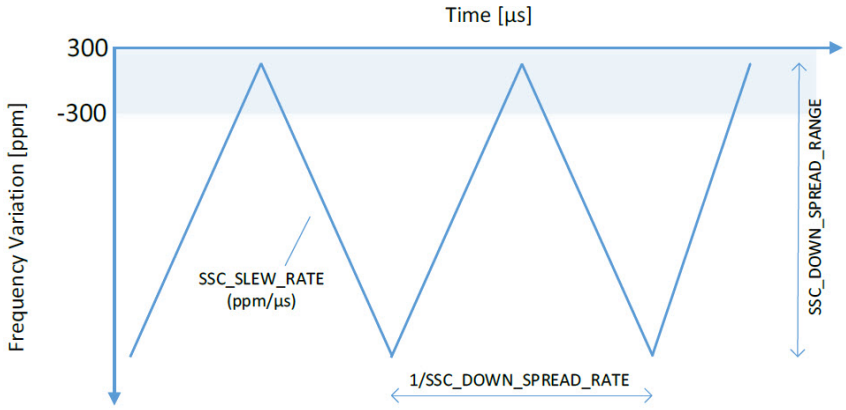


Figure 33 Example Transmitter Frequency During Steady-State

Transmitter Differential Return Loss

Transmitter differential return-loss measurements shall be referenced to a single-ended impedance of 42.5 Ω. When measured at TP2, the differential mode return loss shall not exceed the limits given in the following equation:

$$\mathrm{SDD22(f)} = \begin{cases} -8.5 & 0.05 < f_{GHz} \leq 3 \\ -3.5 + 8.3 \cdot \log 10\left(\frac{f_{GHz}}{12}\right) & 3 < f_{GHz} \leq 12 \end{cases}$$

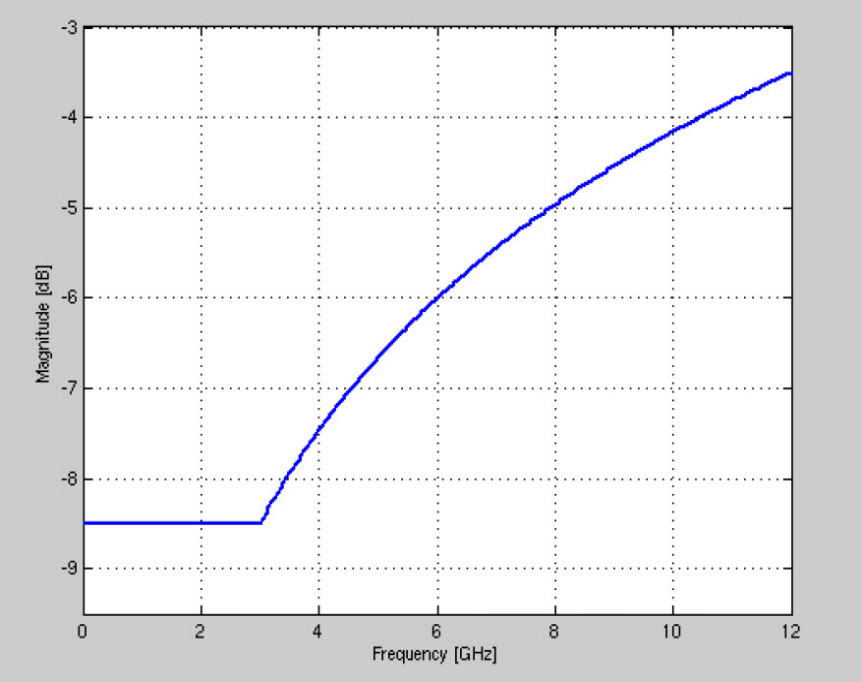


Figure 34 TX Differential Return Loss Mask

Transmitter Common Mode Return Loss

Transmitter common-mode return-loss measurements shall be referenced to a single-ended impedance of 42.5 Ω. When measured at TP2, the common -mode return loss shall not exceed the limits given in the following equation:

$$SCC22(f) = \begin{cases} -6 & 0.05 < f_{GHz} \leq 2.5 \\ -3 & 2.5 < f_{GHz} \leq 12 \end{cases}$$

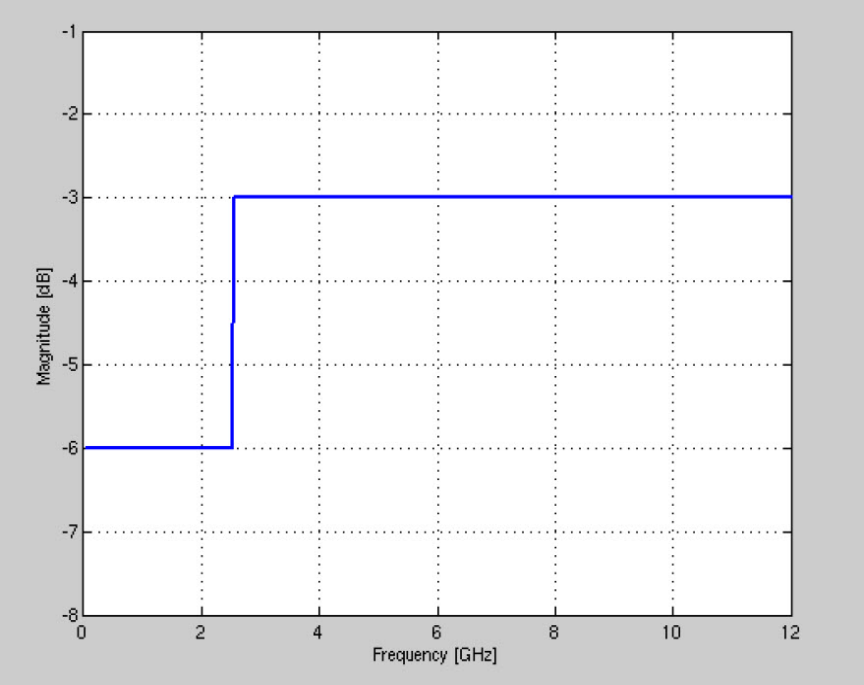


Figure 35 TX Common-Mode Return Loss Mask

Transmit Equalization

A Router Assembly shall support coefficient-based equalization at its transmitter output. The equalizer's structure is based on a 3-tap UI-spaced finite-impulse-response (FIR) filter as shown in Figure 36. The transmitted level corresponding to the nth symbol shall be generated as follows:

$$tx\_out_n = \sum_{k=-1}^{1} data\_in_{n-k} \cdot C_k$$

where:

tx_out_n is the transmitted level at time instant n
$data\_in_{n-k}$ is the data symbol at time instant n-k (may be +1 or -1)
C_k is the k^{th} coefficient of the FIR filter

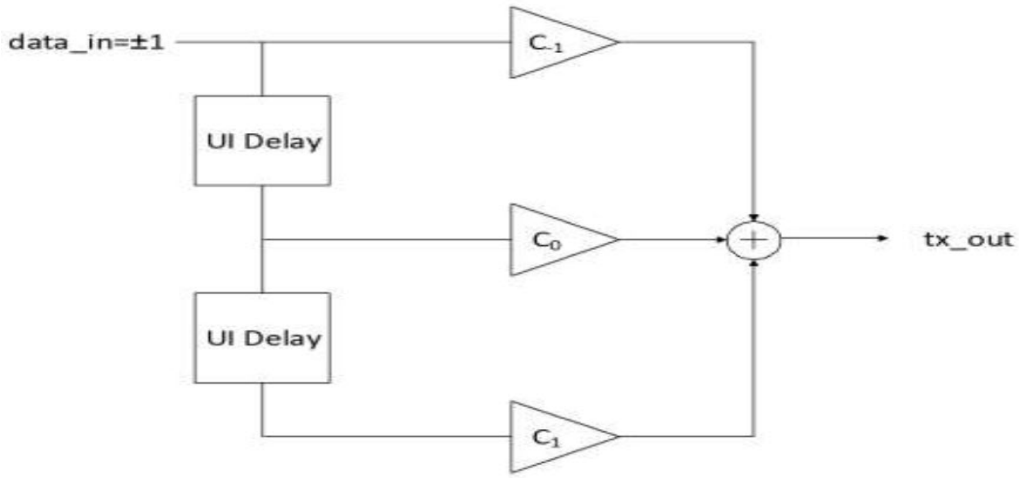


Figure 36 Transmitter Equalizer Structure

Table 5 lists the pre-shoot and de-emphasis transmitter equalization presets that a transmitter shall support. It also includes the corresponding informative coefficients values provided as a reference. Preset configurations 0-14 represent operation mode with full-swing transmitter output, while configuration 15 represent low swing mode. When configuration 15 is selected, the transmitter's output swing shall be attenuated by 3.5 ± 1 dB compared to its full-swing operation. The required tolerance of the pre-shoot and de-emphasis specifications is ± 1 dB.

For each preset, the pre-shoot and de-emphasis shall be measured at TP2 using SQ128 pattern (see Table 8-56 of the USB4 Specification Version 1.0). The pre-shoot shall be calculated as the ratio of the steady-state voltage obtained when configuring the transmitter equalizer such that the pre-cursor tap's magnitude is moved to the main tap, divided by the steady-state voltage with the standard transmit filter configuration. The de-emphasis shall be calculated as the ratio of the steady-state voltage obtained with the standard filter configuration, divided by the steady-state voltage when configuring the transmitter equalizer such that the post -cursor tap's magnitude is moved to the main tap.

Table 5 Transmitter Equalization Presets

Preset Number	Pre-Shoot [dB]	De-Emphasis [dB]	Informative Filter Coefficients		
			C_{-1}	C_0	C_1
0	0	0	0	1	0
1	0	-1.9	0	0.90	-0.10
2	0	-3.6	0	0.83	-0.17
3	0	-5.0	0	0.78	-0.22
4	0	-8.4	0	0.69	-0.31
5	0.9	0	-0.05	0.95	0
6	1.1	-1.9	-0.05	0.86	-0.09
7	1.4	-3.8	-0.05	0.79	-0.16
8	1.7	-5.8	-0.05	0.73	-0.22
9	2.1	-8.0	-0.05	0.68	-0.27
10	1.7	0	-0.09	0.91	0
11	2.2	-2.2	-0.09	0.82	-0.09
12	2.5	-3.6	-0.09	0.77	-0.14
13	3.4	-6.7	-0.09	0.69	-0.22
14	3.8	-3.8	-0.13	0.74	-0.13
15	1.7	-1.7	-0.05	0.55	-0.05

Notes for Table 5**:**

1 The coefficients are normalized such that $|C_{-1}| + C_0 + |C_1|$ corresponds to full output swing. Preset configuration 15 represents operation mode with lower transmitter swing.

2 Preshoot and de-emphasis are calculated as following:

$$Preshoot = 20 \cdot \log 10 \left(\frac{-C_{-1} + C_0 + C_1}{C_{-1} + C_0 + C_1} \right)$$

$$De - emphasis = 20 \cdot \log 10 \left(\frac{C_{-1} + C_0 + C_1}{C_{-1} + C_0 - C_1} \right)$$

Figure 37 and Figure 38 depict the frequency responses of the different transmit equalization presets for Gen 2 and Gen 3 modes of operation, respectively.

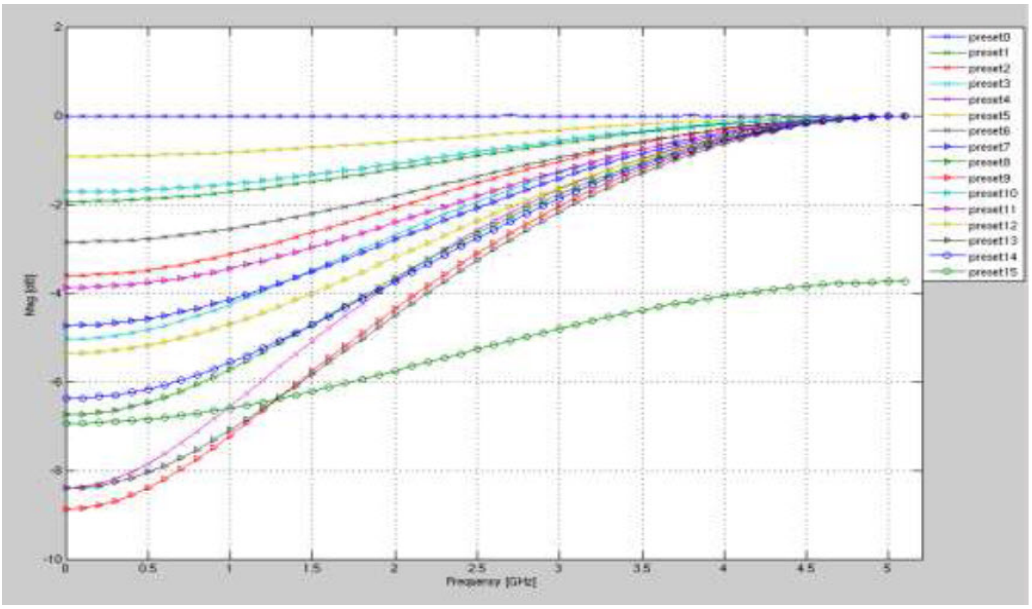


Figure 37 Transmitter Equalization Frequency Response for Gen 2 Systems

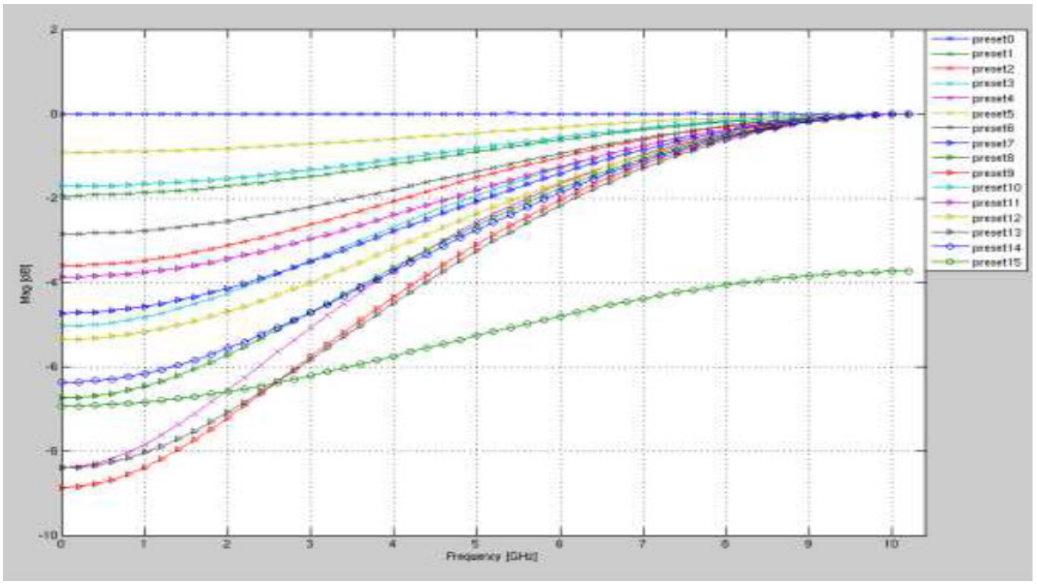


Figure 38 Transmitter Equalization Frequency Response for Gen 3 Systems

Transmitter Compliance Specifications for Gen 2

A transmitter operating in Gen 2 mode shall meet the specifications in Table 3, Table 6, and Table 7.

Table 6 Gen 2 Transmitter Specifications at TP2

Symbol	Description	Min	Max	Units	Comments
UI	Minimum Unit Interval	99.97	100.03	ps	The minimum UI value corresponds to the Link baseline speed of 10.0 Gbps with an uncertainty range of -300 ppm to 300 ppm. See Note 4.
AC_CM	TX AC Common Mode voltage	---	100	mV pp	
TJ	Total Jitter	---	0.38	UI pp	See Note 2 and Note 3
UJ	Sum of uncorrelated DJ and RJ components (all jitter components except for DDJ)	---	0.31	UI pp	See Note 2
DDJ	Data-Dependent Jitter	---	0.15	UI pp	See Note 5
UDJ	Deterministic jitter that is uncorrelated to the transmitted data	---	0.17	UI pp	
UDJ_LF	Low Frequency Uncorrelated Deterministic Jitter	---	0.04	UI pp	See Note 6
DCD	Even-odd jitter associated with Duty-Cycle-Distortion	---	0.03	UI pp	
Y1	TX eye inner height (one-sided voltage opening of the differential signal)	140	---	mV	Measured for 1E6 UI. See Note 1, Note 2, and Figure 39.
Y2	TX eye outer height (one-sided voltage opening of the differential signal)	---	650	mV	Measured for 1E6 UI. See Note 1, Note 2, and Figure 39.

Notes for Table 6:

1. TX voltage is differential.

2. Measured while applying the reference CDR described in Section “Reference Clock-and-Data-Recovery (CDR) Function”. Note that the measured jitter includes residual SSC jitter passing the reference CDR.

3. TJ is defined as the sum of all “deterministic” components plus 14.7 times the RJ RMS (the transmitter RJ RMS multiplier corresponds to the target BER with some margin on top).

4. UI shall be calculated dynamically using a uniform moving average filter with window size of 3000 symbols.

5. The transmit equalization shall be set such that the data dependent jitter is minimized.

6. UDJ_LF is the uncorrelated deterministic jitter measured after applying a 2^{nd} order Low-Pass-Filter with 3 dB cut-off at 0.5 MHz on the measured jitter. This filter needs to be applied on top of the reference CDR function described in Section “Reference Clock-and-Data-Recovery (CDR) Function”.

Table 7 Gen 2 Transmitter Specifications at TP3

Symbol	Description	Min	Max	Units	Comments
TJ	Total Jitter	---	0.60	UI pp	See Note 2, Note 3
UJ	Sum of uncorrelated DJ and RJ components (all jitter components except for DDJ)	---	0.31	UI pp	Note 2
UDJ	Deterministic jitter that is uncorrelated to the transmitted data	---	0.17	UI pp	
X1	TX eye horizontal deviation	---	0.24	UI	Measured for 1E6 UI. See Note 2, Note 4, and Figure 39
Y1	TX eye inner height (one-sided voltage opening of the differential signal)	47	---	mV	Measured for 1E6 UI. See Note 1, Note 2, and Figure 39
Y2	TX eye outer height (one-sided voltage opening of the differential signal)	---	650	mV	Measured for 1E6 UI. See Note 1, Note 2, and Figure 39

Notes for Table 7:

1 TX voltage is differential.

2 Measured while applying the reference CDR described in Section “Reference Clock-and-Data-Recovery (CDR) Function” and the reference equalizer defined in Section “Reference Equalization Function”. Note that the measured jitter includes residual SSC jitter passing the reference CDR.

3 TJ is defined as the sum of all “deterministic” components plus 14.7 times the RJ RMS (the transmitter RJ RMS multiplier corresponds to the target BER with some margin on top).

4 X1 specification is informative but shall be assumed as a valid reference if direct TJ measurement cannot be reliably performed.

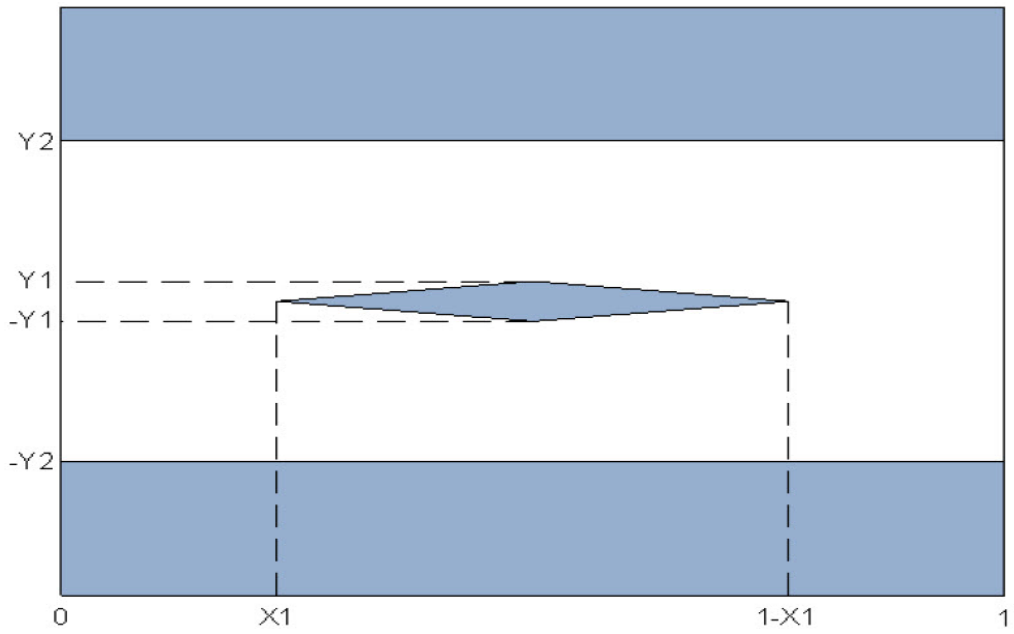


Figure 39 TX Mask Notations

Transmitter Compliance Specifications for Gen 3 Interconnects

A transmitter operating in Gen 3 mode shall meet the specifications in Table 3, Table 8, and Table 9.

Table 8 Gen 3 Transmitter Specifications at TP2

Symbol	Description	Min	Max	Units	Comments
UI	Minimum Unit Interval	49.985	50.015	ps	The minimum UI value corresponds to the Link baseline speed of 20.0 Gbps with an uncertainty range of -300 ppm to 300 ppm. See Note 4.
AC_CM	TX AC Common Mode voltage	---	100	mV pp	
TJ	Total Jitter	---	0.46	UI pp	See Note 2 and Note 3
UJ	Sum of uncorrelated DJ and RJ components (all jitter components except for DDJ)	---	0.31	UI pp	See Note 2
DDJ	Data-Dependent Jitter	---	0.21	UI pp	See Note 5
UDJ	Deterministic jitter that is uncorrelated to the transmitted data	---	0.17	UI pp	
UDJ_LF	Low Frequency Uncorrelated Deterministic Jitter	---	0.07	UI pp	See Note 6

Symbol	Description	Min	Max	Units	Comments
DCD	Even-odd jitter associated with Duty-Cycle-Distortion	---	0.03	UI pp	
Y1	TX eye inner height (one-sided voltage opening of the differential signal)	120	---	mV	Measured for 1E6 UI. See Note 1, Note 2, and Figure 39.
Y2	TX eye outer height (one-sided voltage opening of the differential signal)	---	650	mV	Measured for 1E6 UI. See Note 1, Note 2, and Figure 39.

Notes for Table 8:

1. TX voltage is differential.

2. Measured while applying the reference CDR described in Section “Reference Clock-and-Data-Recovery (CDR) Function”. Note that the measured jitter includes residual SSC jitter passing the reference CDR.

3. TJ is defined as the sum of all “deterministic” components plus 14.7 times the RJ RMS (the transmitter RJ RMS multiplier corresponds to the target BER with some margin on top).

4. UI shall be calculated dynamically using a uniform moving average filter with window size of 3000 symbols.

5. The transmit equalization shall be set such that the data dependent jitter is minimized.

6. UDJ_LF is the uncorrelated deterministic jitter measured after applying a 2^{nd} order Low-Pass-Filter with 3 dB cut-off at 0.5 MHz on the measured jitter. This filter needs to be applied on top of the reference CDR function described in Section “Reference Clock-and-Data-Recovery (CDR) Function”.

Table 9 Gen 3 Transmitter Specifications at TP3

Symbol	Description	Min	Max	Units	Comments
TJ	Total Jitter	---	0.60	UI pp	See Note 2, Note 3
UJ	Sum of uncorrelated DJ and RJ components (all jitter components except for DDJ)	---	0.31	UI pp	Note 2
UDJ	Deterministic jitter that is uncorrelated to the transmitted data	---	0.17	UI pp	
X1	TX eye horizontal deviation	---	0.23	UI	Measured for 1E6 UI. See Note 2, Note 4, and Figure 39
Y1	TX eye inner height (one-sided voltage opening of the differential signal)	49	---	mV	Measured for 1E6 UI. See Note 1, Note 2, and Figure 39
Y2	TX eye outer height (one-sided voltage opening of the differential signal)	---	650	mV	Measured for 1E6 UI. See Note 1, Note 2, and Figure 39

Notes for Table 9:

1 TX voltage is differential.

2 Measured while applying the reference CDR described in Section “Reference Clock-and-Data-Recovery (CDR) Function” and the reference equalizer defined in Section

"Reference Equalization Function". Note that the measured jitter includes residual SSC jitter passing the reference CDR.

3 TJ is defined as the sum of all "deterministic" components plus 14.7 times the RJ RMS (the transmitter RJ RMS multiplier corresponds to the target BER with some margin on top).

4 X1 specification is informative but shall be assumed as a valid reference if direct TJ measurement cannot be reliably performed.

5 Transmitter Tests for 10.3125 GB/s Systems

Tx Preset Calibration / 91
SBTX High Voltage / 94
SBTX Low Voltage / 96
SBTX Rise/Fall Time / 98
SBTX UI Duration / 101
SBRX High Voltage Detection / 104
SBRX Low Voltage Detection / 106
TX Rise/Fall Time / 107
Tx Uncorrelated Jitter / 109
Tx Uncorrelated Deterministic Jitter / 111
Tx Data Dependent Jitter / 113
Tx Duty Cycle Distortion / 115
Tx Low Frequency Uncorrelated Deterministic Jitter / 117
Tx Total Jitter / 119
Tx Uncorrelated Jitter TP3 / 121
Tx Uncorrelated Deterministic Jitter TP3 / 123
Tx Total Jitter TP3 / 125
Tx Eye Diagram TP3 / 128
Tx Average Unit Interval, Min/Max / 131
Tx Minimum Unit Interval, Min/Max / 133
Tx SSC Down Spread Rate / 135
Tx SSC Down Spread Range / 137
Tx SSC Slew Rate / 139
Tx SSC Phase Deviation / 141
Tx Eye Diagram / 143
Tx AC Common Mode Voltage / 146
Tx Equalization Tests / 148
Tx Electrical Idle Voltage Test / 154
Tx Differential Return Loss Test / 156
Tx Common Mode Return Loss Test / 161
Rx Differential Return Loss Test / 166
Rx Common Mode Return Loss Test / 171

This section provides the Methods of Implementation (MOIs) to run electrical tests on a USB DUT operating at a bit rate of 10.3125 GB/s using an Keysight Infiniium Oscilloscope and other accessories, along with the USB4 Test Application.

KEYSIGHT TECHNOLOGIES

NOTE All USB4 devices that support a bit rate of 10.3125 Gb/s are classified as Gen2 devices.

Tx Preset Calibration

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Preset Calibration Test is to find the optimized preset for the platform.

NOTE Prior to running the compliance tests, the Host / Device must go through Preset Calibration.

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 41 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Preset Calibration* are checked.

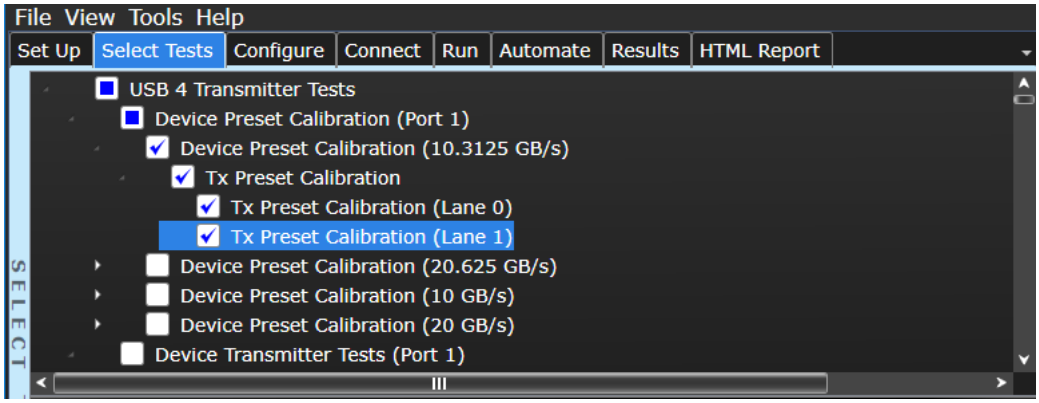


Figure 40 Selecting the Tx Preset Calibration tests

NOTE By default, the test group for **Preset Calibration** for each selected bit-rate is hidden in the **Select Tests** tab when **Predefined Optimum Preset Number** is selected for the respective bit-rates. To view and select the **Preset Calibration** tests in the **Select Tests** tab, select the **Run Preset Calibration** option in the **Test Setup** window of the **Set Up** tab.

NOTE

In the **Measurement Server** mode or **Multi** instance mode, it is recommended to run the **Tx Preset Calibration** tests first to get the optimized preset value. Then use this value to run the remaining transmitter tests.

Detailed Process:

In the **Measurement Server** mode or **Multi** instance mode, after running the **Preset Calibration** test, please see the HTML Report and note down the optimized preset value. Then, please navigate to **Set Up** tab > **Test Setup** button > **Test Setup** dialog box. Select the check box "Predefined Optimum Preset Number", use the already noted optimized preset number, and manually **Select the Optimum Preset Number for Each Bit Rate**. Now, please run the rest of the transmitter tests.

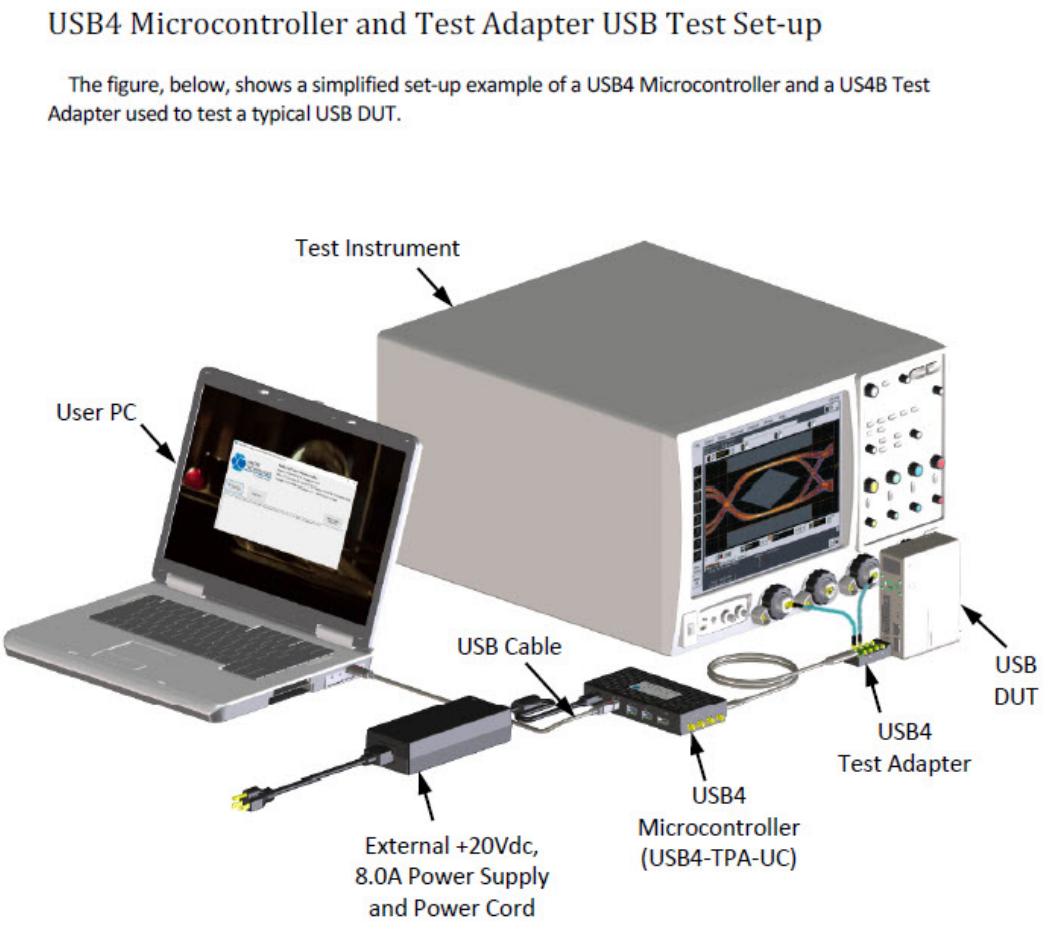


Figure 41 Transmitter TP2/TP3 Test Setup

Test Procedure

1 Connect the DUT to the Oscilloscope as shown in the Figure 41.
2 Choose a USB4 speed to start with.
3 Configure the DUT transmitter to output PRBS15, preset 0 on all lanes with SSC enabled.
4 The cables from the plug test fixture to the scope shall be de-embedded.
5 Perform measurements with:
   a Reference CDR modeled by a 2nd order PLL response which drives High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used.
   b Oscilloscope with a minimum bandwidth of 16 GHz.
6 Capture the waveform and process it with the digital oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Evaluate 40 Mpts per channel when using 80 GSa/s. For higher sample rate use memory depth in the same ration to 40 Mpts.
   c Pattern length - Periodic
   d Jitter separation method shall be suitable for cross talk on signal
   e Adjust vertical scale to fit signal into scope screen.
   f Referenced to 1E-13 statistics.
7 Capture DDJ results for lane 0.
8 Repeat the test for all remaining USB4 transmit presets (till preset 15 as shown in Table 5).
9 Repeat the test for the remaining USB4 lanes.
10 For each lane, choose the preset that provides minimum DDJ.
11 Repeat the above procedure for all supported USB4 speeds.

Expected / Observable Results

For each lane, the preset that provides the minimum DDJ is the optimized preset for the platform.

Test References

See

- *Universal Serial Bus 4 (USB Type-C) Specification Version 2.00 (Table 3-5)*

SBTX High Voltage

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of this test is to confirm that the SBTX High Voltage Measurement of a USB4 device is within the specification limits.

Test Pass Requirement

2.40 V ≤ SBTX High Voltage Measurement ≤ 3.52 V

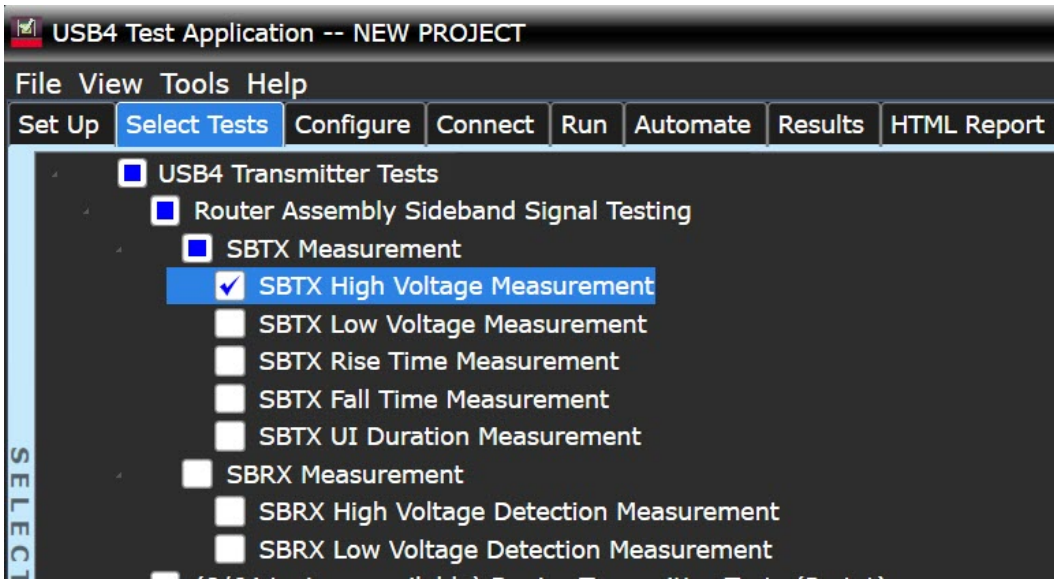
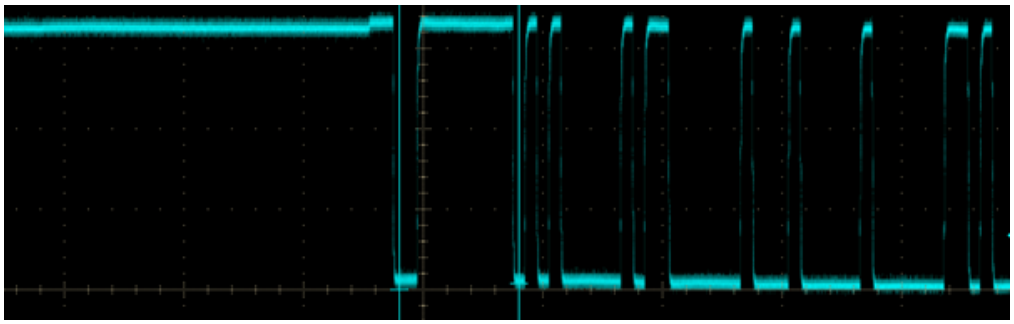


Figure 42 Selecting the SBTX High Voltage Measurement test

Test Procedure

1. Connect a voltage meter/DMMfluke to SBU1 header in the USB4 Test Fixture.
2. Power up the DUT.
3. Measure the voltage.
4. If $SBTX_{VOH}$ < 2.4 V or > 3.52 V then Fail.
5. Connect a scope with high impedance probe to the SBU1 header in the USB4 Test Fixture.
6. In the scope use a trigger based on pulse width, negative polarity, trigger when the pulse width <10 µs and threshold of 600 mV.
7. Horizontal scale = 10 µs per square, vertical scale = 1 V per square.
8. Power up the DUT.

9 Over the Infiniium Oscilloscope the trigger shall capture the transaction pattern.



10 Measure the high/low value of the "1" amplitude for a bit inside the transaction. Over/undershoot shall be ignored.

11 If $SBTX_{VOH}$ < 2.4 V or > 3.52 V then Fail.

Expected / Observable Results

If $SBTX_{VOH}$ < 2.4 V or > 3.52 V then Fail.

Test References

See

- *USB4 Specification Version 2.00 (Table 3-32)*

SBTX Low Voltage

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of this test is to confirm that the SBTX Low Voltage Measurement of a USB4 device is within the specification limits.

Test Pass Requirement

2.40 V ≤ SBTX Low Voltage Measurement ≤ 3.52 V

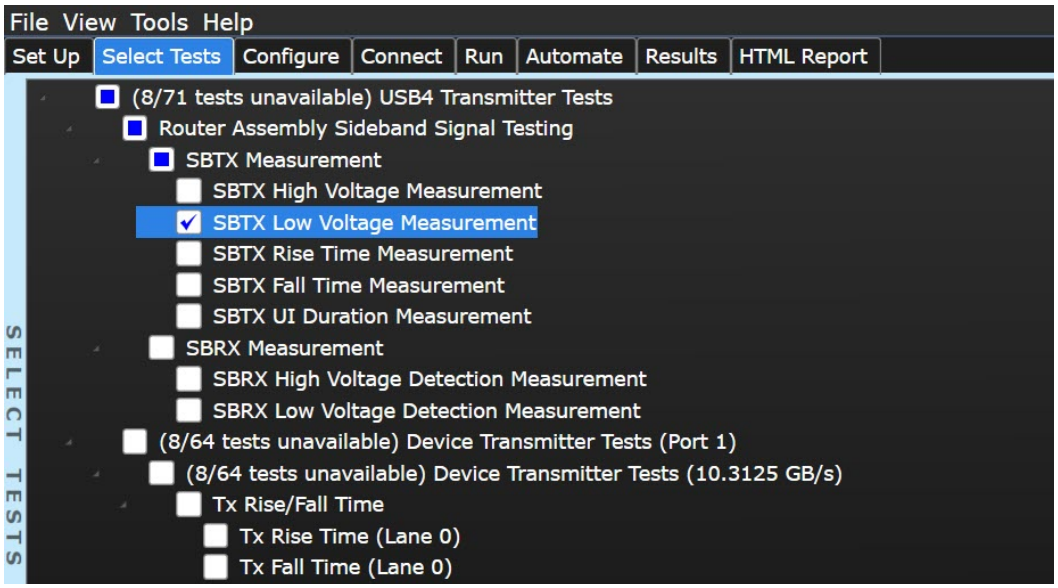


Figure 43 Selecting the SBTX Low Voltage Measurement test

Test Procedure

1. Connect a voltage meter/DMMfluke to SBU1 header in the USB4 Test Fixture.
2. DUT shall be in power down state.
3. Measure the voltage.
4. If $SBTX_{VOL}$ < -0.05 V or > 0.4 V then Fail.
5. Connect a scope with high impedance probe to the SBU1 header in the USB4 Test Fixture.
6. In the scope use a trigger based on pulse width, negative polarity, trigger when the pulse width <10 µs and threshold of 600 mV.
7. Horizontal scale = 10 µs per square, vertical scale = 1 V per square.
8. Connect link partner to the DUT.
9. Over the Infiniium Oscilloscope the trigger shall capture the transaction pattern.

10 Measure the high/low value of the "0" amplitude for a bit inside the transaction. Over/undershoot shall be ignored.

11 If $SBTX_{VOL}$ < -0.05 V or > 0.4 V then Fail.

Expected / Observable Results

If $SBTX_{VOL}$ < -0.05 V or > 0.4 V then Fail.

Test References

See

- *USB4 Specification Version 2.00 (Table 3-32)*

SBTX Rise/Fall Time

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of this test is to confirm that the SBTX Rise/Fall Time Measurement of a USB4 device is within the specification limits.

Test Pass Requirement

$3.5\ ns \leq SBX_{TRTF} \leq 65\ ns$.

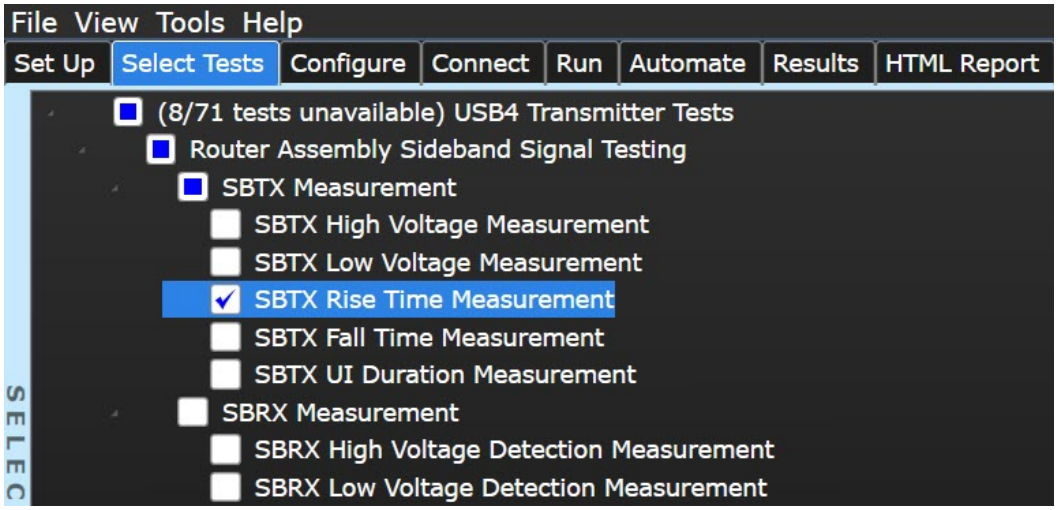


Figure 44 Selecting the SBTX Rise Time Measurement test

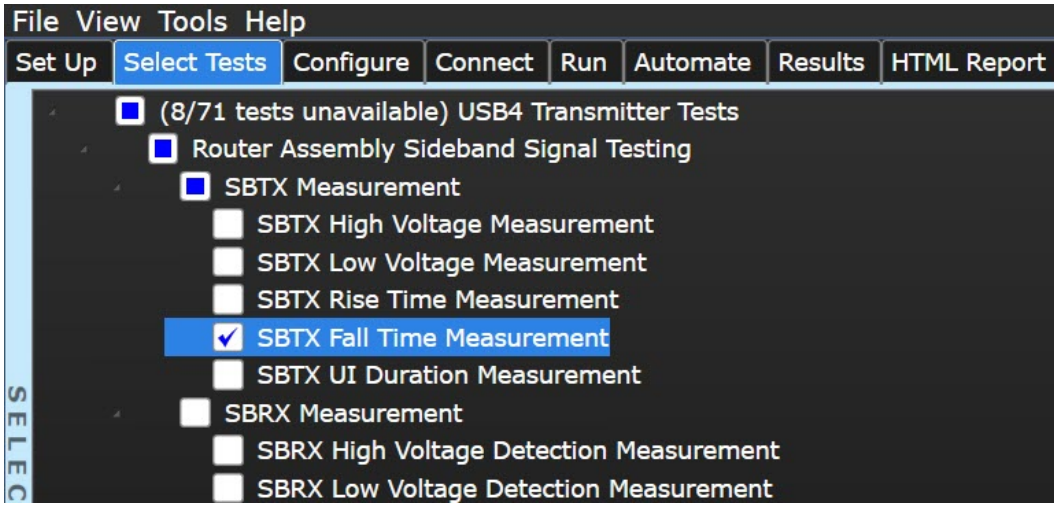
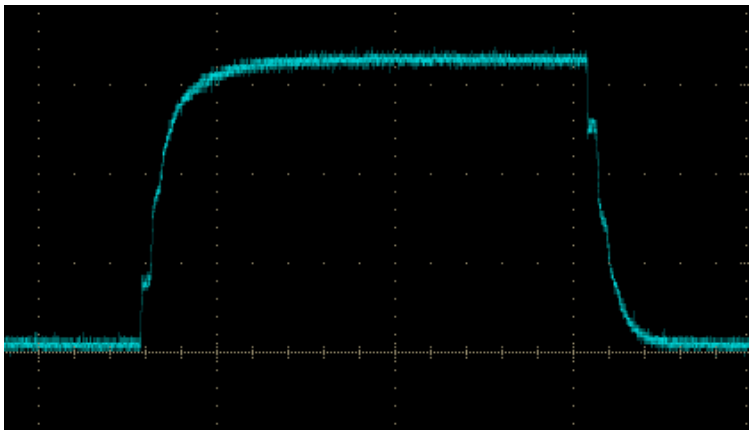


Figure 45 Selecting the SBTX Fall Time Measurement test

Test Procedure

1 Connect the DUT via USB4 Test Fixture with USB4 u-controller in order to establish link.
2 The measurement shall be in transaction only and not from power down to up (or the opposite).
3 Connect a scope with high impedance probe to the SBU1 header for SBTX test in the USB4 Test Fixture.
4 In the scope use a trigger based on pulse width, negative polarity, trigger when the pulse width <10 µs and threshold of 600 mV.
5 Horizontal scale = 10 µs per square, vertical scale = 1 V per square.
6 Power up the DUT.
7 Over the Infiniium Oscilloscope the trigger shall capture the transaction pattern.
8 Zoom in one bit from inside the transaction pattern. Not the 1st or the last bit.



9 Measure the rise and fall time (10%-90%) for SBTX.
10 If 65 ns < STX_{TRTF} < 3.5 ns then Fail.

Expected / Observable Results

If 65 ns < STX_{TRTF} < 3.5 ns then Fail.

Test References

See

- *USB4 Specification Version 2.00 (Table 3-32)*

SBTX UI Duration

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of this test is to confirm that the SBTX UI Duration Measurement of a USB4 device is within the specification limits.

Test Pass Requirement

970 ns ≤ SBX_{UI} ≤ 1030 ns.

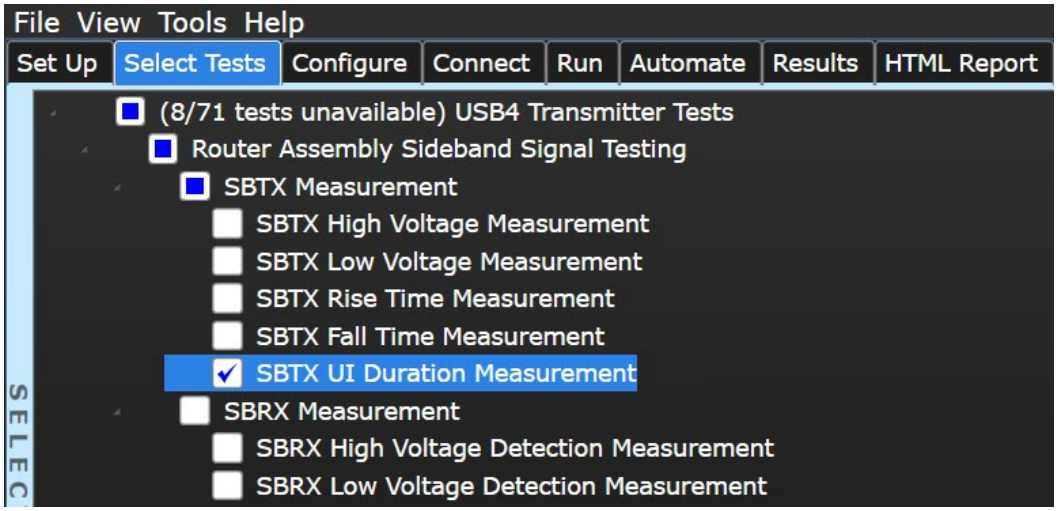
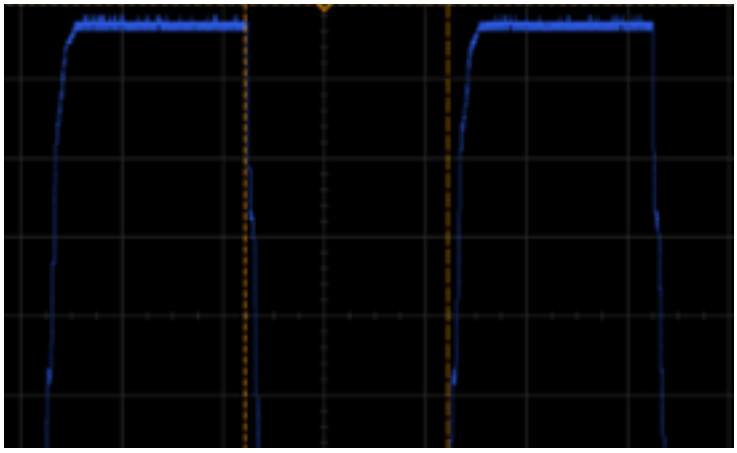


Figure 46 Selecting the SBTX UI Duration Measurement test

Test Procedure

1 Connect the DUT via USB4 Test Fixture with USB4 u-controller in order to establish link.
2 The measurement shall be in transaction only, over the transaction pattern.
3 Connect a scope with high impedance probe to the SBU1 header for SBTX test in the USB4 Test Fixture.
4 In the scope use a trigger based on pulse width, negative polarity, trigger when the pulse width <10 µs and threshold of 600 mV.
5 Horizontal scale = 10 µs per square, vertical scale = 1 V per square.
6 Power up the DUT.
7 Over the Infiniium Oscilloscope the trigger shall capture the transaction pattern.
8 Zoom in "10" bits from the transaction pattern.



9 Measure the duration from falling edge of the "1" to the rising edge of "0", named SBX_UI.
10 If 970 ns < $SBTX_{UI}$ < 1030 ns then Fail.

Expected / Observable Results

If 970 ns < $SBTX_{UI}$ < 1030 ns then Fail.

Test References

See

- *USB4 Specification Version 2.00 (Table 3-32)*

SBRX High Voltage Detection

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of this test is to confirm that the SBRX High Voltage Detection Measurement of a USB4 device is within the specification limits.

Test Pass Requirement

$2.0\ V \leq SBRX_{VIH} \leq 3.77\ V$

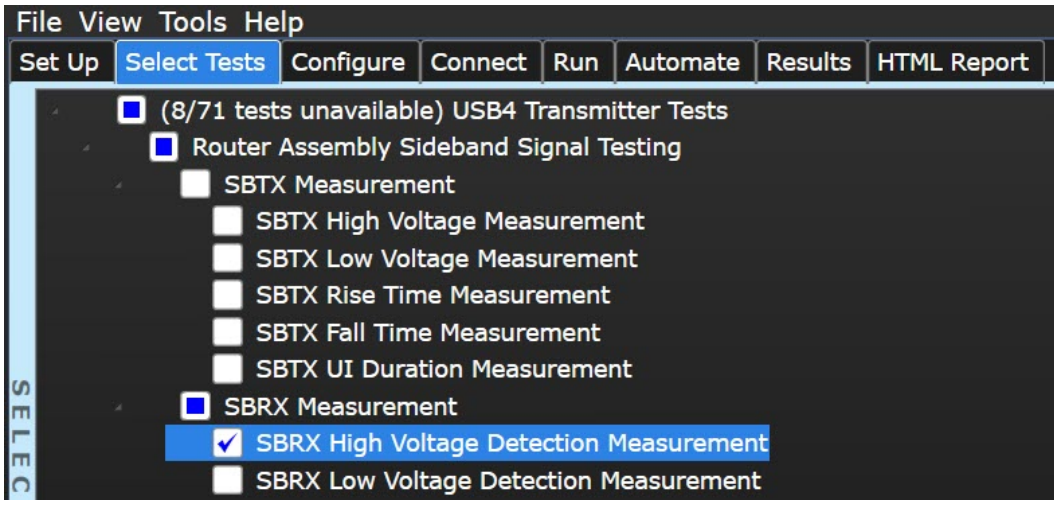
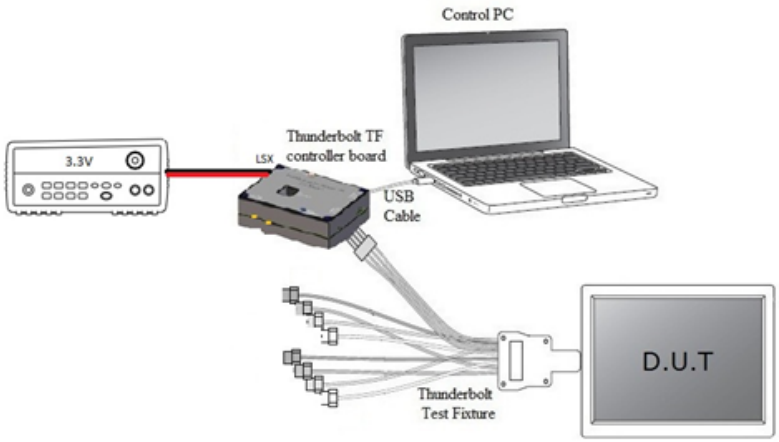


Figure 47 Selecting the SBRX High Voltage Measurement test

Test Procedure

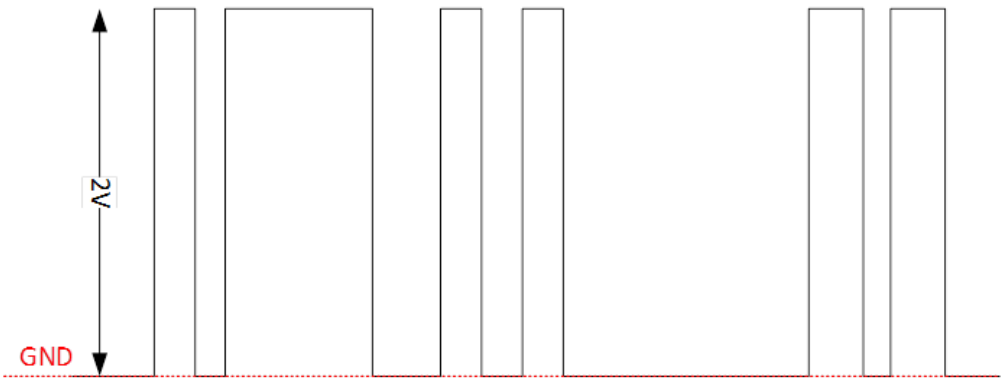
1 Connect the DUT via USB4 LSXX Test Fixture with USB4 u-controller and set '1' bit amplitude to 3.3 V and '0' bit amplitude to 0 V in order to establish link.



2 Set the 3.3 V power supply to 3.77 V.

3 Establish there is a link.

4 Reduce the external power supply to 2.0 V.



5 If link is lost, then Fail.

Expected / Observable Results

2.0 V ≤ $SBRX_{VIH}$ ≤ 3.77 V

Test References

See

- *USB4 Specification Version 2.00 (Table 3-32)*

SBRX Low Voltage Detection

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of this test is to confirm that the SBRX Low Voltage Detection Measurement of a USB4 device is within the specification limits.

Test Pass Requirement

$-0.3\ V \leq SBRX_{VIL} \leq 0.65\ V$

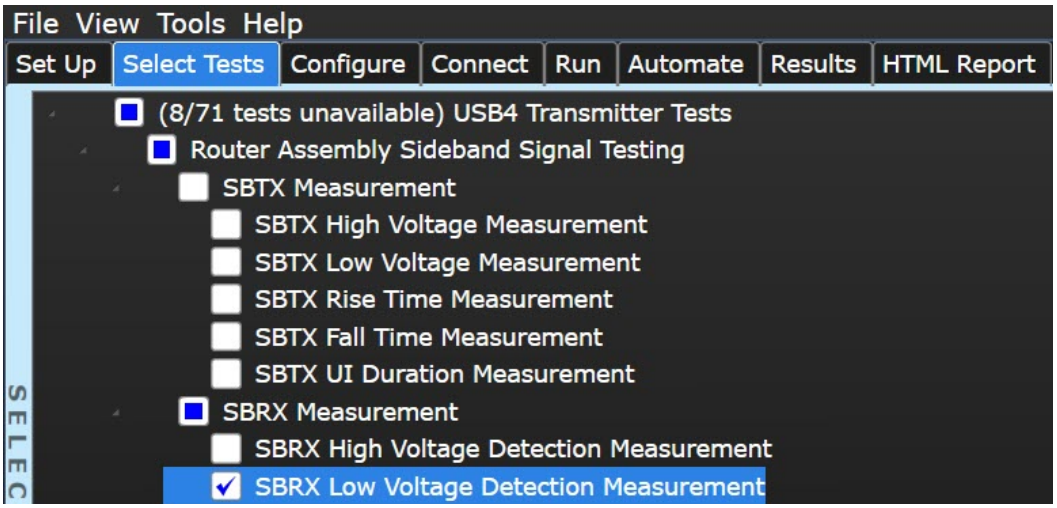


Figure 48 Selecting the SBRX Low Voltage Measurement test

Test Procedure

1. Connect the DUT via USB4 Test Fixture with USB4 u-controller with external 3.3 V power supply connected to the SBX input in order to establish link.
2. Set the 3.3 V power supply to 3.3 V.
3. Establish there is a link.
4. Reduce the external power supply to 0.65 V.
5. If link is established, then Fail.

Expected / Observable Results

$-0.3\ V \leq SBRX_{VIL} \leq 0.65\ V$

Test References

See

- *USB4 Specification Version 2.00 (Table 3-32)*

TX Rise/Fall Time

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Rise/Fall Time Test is to confirm that the rise times and fall times on the USB differential signals are within the limits of the specification.

Test Pass Requirement

Rise Time and Fall Time $\geq$ 10.00 ps (Refer to Table 3 on page 74).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 41 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Rise/Fall Time* are checked.

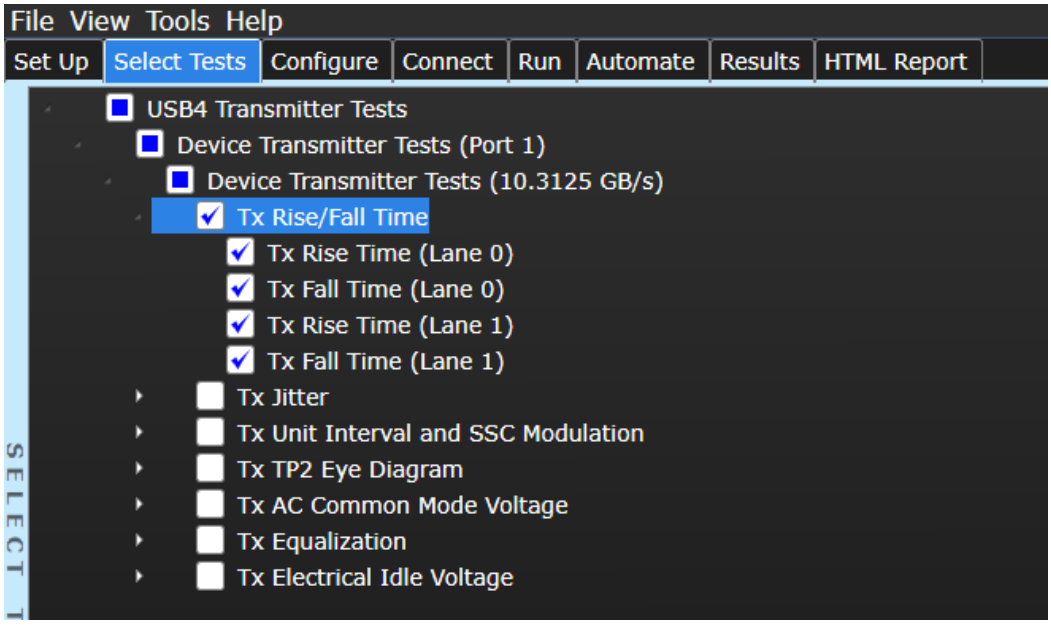


Figure 49 Selecting the Tx Rise/Fall Time tests

Test Procedure

1. Configure DUT transmitter to output alternating square pattern of 64 0's and 64 1's (SQ128) on all lanes with SSC turned on.
2. Evaluate at least 4Mpts per channel when using 80 GSa/s. For higher sample rates, use memory depth in the same ratio to 4Mpts. Use the maximum analog bandwidth of the Oscilloscope.

   No CDR, no average and no interpolation to be used.

   Adjust vertical scale such that the signal fits within the Oscilloscope's display.
3. Measure T_{RISE} as the mode of the sampled edge times from 20% to 80% of the differential swing voltage rising edge.
4. Measure T_{FALL} as the mode of the sampled edge times from 80% to 20% of the differential swing voltage falling edge.
5. Repeat the test for the remaining USB lanes.

Expected / Observable Results

If $T_{RISE} < 10$ ps, the status of test is FAIL.

If $T_{FALL} < 10$ ps, the status of test is FAIL.

Test References

See

- *USB4 Specification Version 2.00 (Table 3-2)*

Tx Uncorrelated Jitter

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Uncorrelated Jitter Test is to confirm that the Uncorrelated Jitter [Deterministic Jitter (DJ) and Random Jitter (RJ) components] of the transmitter is within the limits of the specification.

Test Pass Requirement

Uncorrelated Jitter (UJ) $\leq$ 0.31 UI_{p-p} (Refer to Table 6 on page 83).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 41 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter, Data Dependent Jitter and Duty Cycle Distortion* are checked.

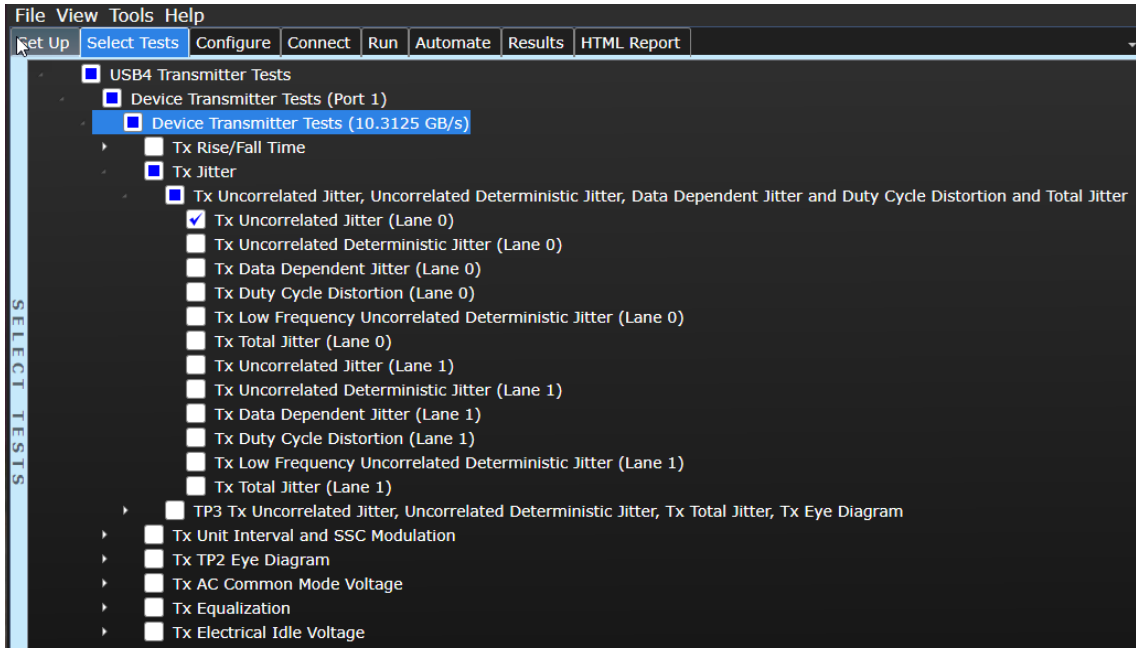


Figure 50 Selecting the Tx Uncorrelated Jitter tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2 Perform measurements with:
   a Reference CDR based on the 2^{nd} order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   b Oscilloscope with a minimum bandwidth of 16GHz
3 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Pattern length – Periodic
   c Jitter Separation method must be suitable for cross-talk on the signal
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Evaluate 40 Mpts per channel when using 80 GSa/s. For higher sample rates, use memory depth in the same ratio to 40 Mpts
   f Referenced to 1E-13 statistics
4 Capture the Total Jitter (TJ) and Data Dependent Jitter (DDJ) results.
5 Calculate UJ using the equation:

$$UJ = TJ - DDJ$$

6 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If UJ > 0.31 UI_{p-p}, the status of test is FAIL.

Test References

See

- *USB4 Specification Version 2.00 (Table 3-5)*

Tx Uncorrelated Deterministic Jitter

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Uncorrelated Deterministic Jitter Test is to confirm that the Uncorrelated Deterministic Jitter of the transmitter is within the limits of the specification.

Test Pass Requirement

Deterministic Jitter that is uncorrelated to the transmitted data (UDJ) $\leq$ 0.17 UI_{p-p} (Refer to Table 6 on page 83).

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see Figure 41 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.
2. Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.
3. Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter, Data Dependent Jitter and Duty Cycle Distortion* are checked.

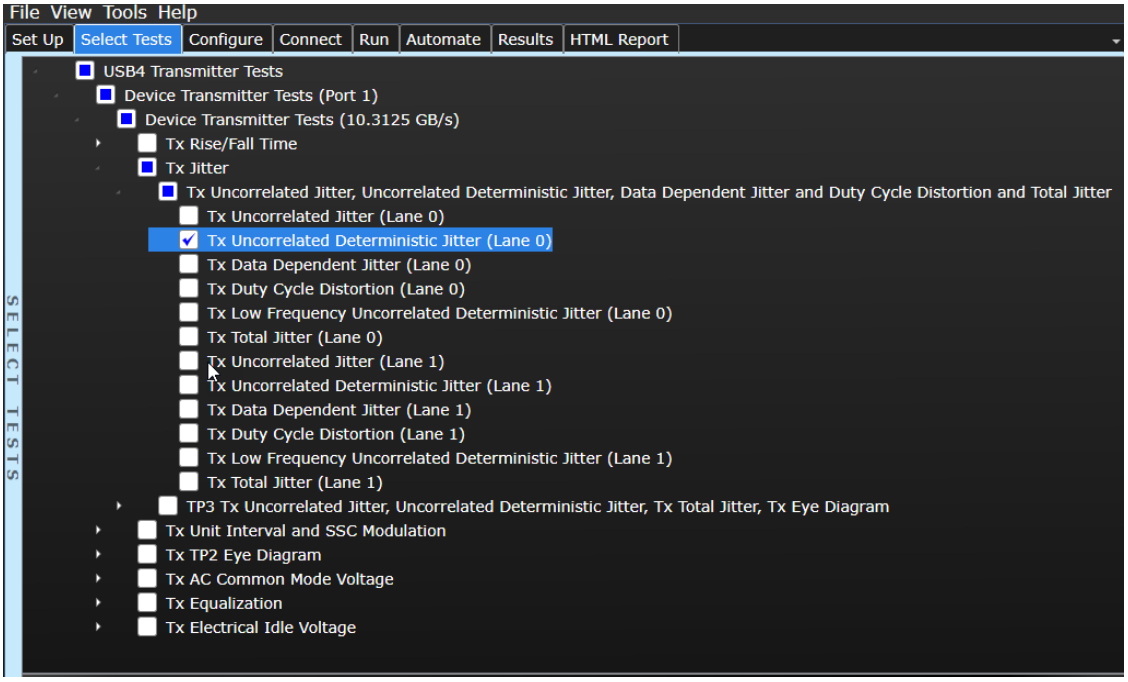


Figure 51 Selecting the Tx Uncorrelated Deterministic Jitter tests

Test Procedure

1. Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2. Perform measurements with:
   a. Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   b. Oscilloscope with a minimum bandwidth of 16 GHz
3. Capture the waveform and process it with the Digital Oscilloscope:
   a. Sampling Rate $\geq$ 80 GSa/s
   b. Pattern length – Periodic
   c. Jitter Separation method must be suitable for cross-talk on the signal
   d. Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e. Evaluate 40 Mpts per channel when using 80 GSa/s. For higher sample rates, use memory depth in the same ratio to 40 Mpts
   f. Referenced to 1E-13 statistics
4. Capture the UDJ result (same as BUJ over the Oscilloscope).
5. Repeat the test for the remaining USB lanes.

Expected / Observable Results

If UDJ > 0.17 UI_{p-p}, the status of test is FAIL.

Test References

See

- *USB4 Specification Version 2.00 (Table 3-5)*

Tx Data Dependent Jitter

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Data Dependent Jitter Test is to confirm that the sum of Data Dependent Jitter (DDJ) of a USB4 device must be less than the maximum limit as per the specification.

Test Pass Requirement

Data Dependent Jitter (DDJ) $\leq$ 0.15 UI_{p-p} (Refer to Table 6 on page 83).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 41 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter, Data Dependent Jitter and Duty Cycle Distortion* are selected.

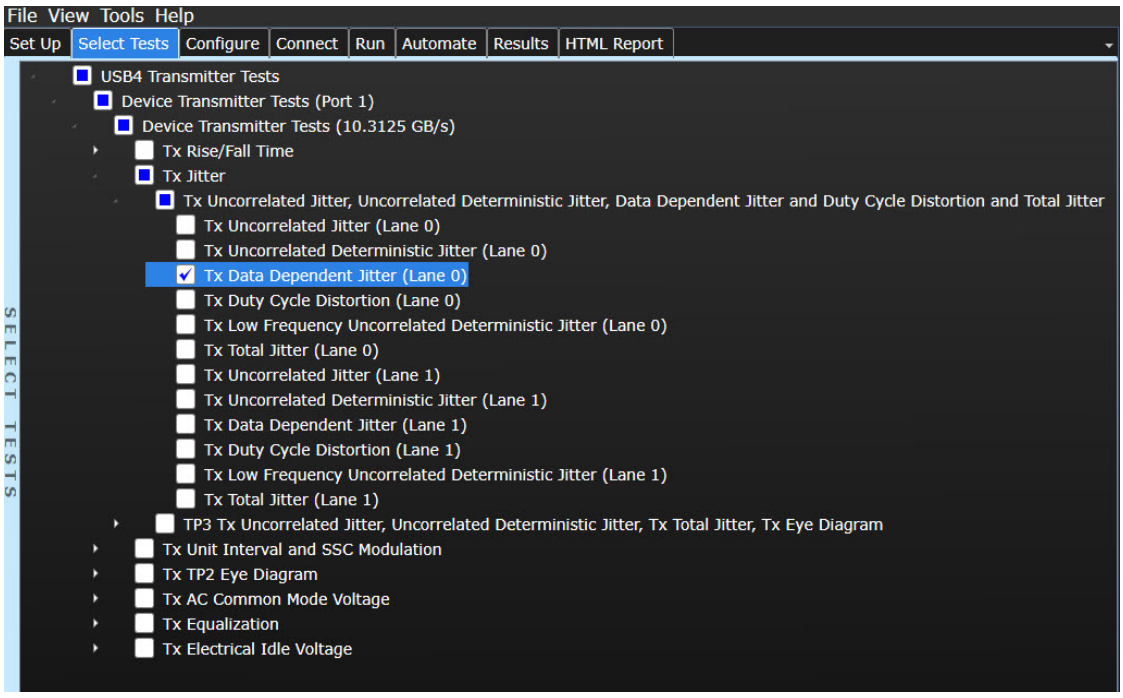


Figure 52 Selecting the Tx Data Dependent Jitter tests

Test Procedure

1. Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2. Perform measurements with:
   a. Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   b. Oscilloscope with a minimum bandwidth of 16 GHz
3. Capture the waveform and process it with the Digital Oscilloscope:
   a. Sampling Rate $\geq$ 80 GSa/s
   b. Pattern length – Periodic
   c. Jitter Separation method must be suitable for cross-talk on the signal
   d. Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e. Evaluate 40 Mpts per channel when using 80 GSa/s. For higher sample rates, use memory depth in the same ratio to 40 Mpts
   f. Referenced to 1E-13 statistics
4. Capture the DDJ result (same as ISI over the Oscilloscope).
5. Repeat the test for the remaining USB lanes.

Expected / Observable Results

If DDJ > 0.15 UI_{p-p}, the status of test is FAIL.

Test References

See

- *USB4 Specification Version 2.00 (Table 3-5)*

Tx Duty Cycle Distortion

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Duty Cycle Distortion Test is to confirm that the transmitter Deterministic Jitter Associated by Duty-Cycle-Distortion Jitter falls within the limits of the specification.

Test Pass Requirement

Duty-Cycle-Distortion (DCD) ≤ 0.03 UIp-p (Refer to Table 6 on page 83).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 41 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter, Data Dependent Jitter and Duty Cycle Distortion* are checked.

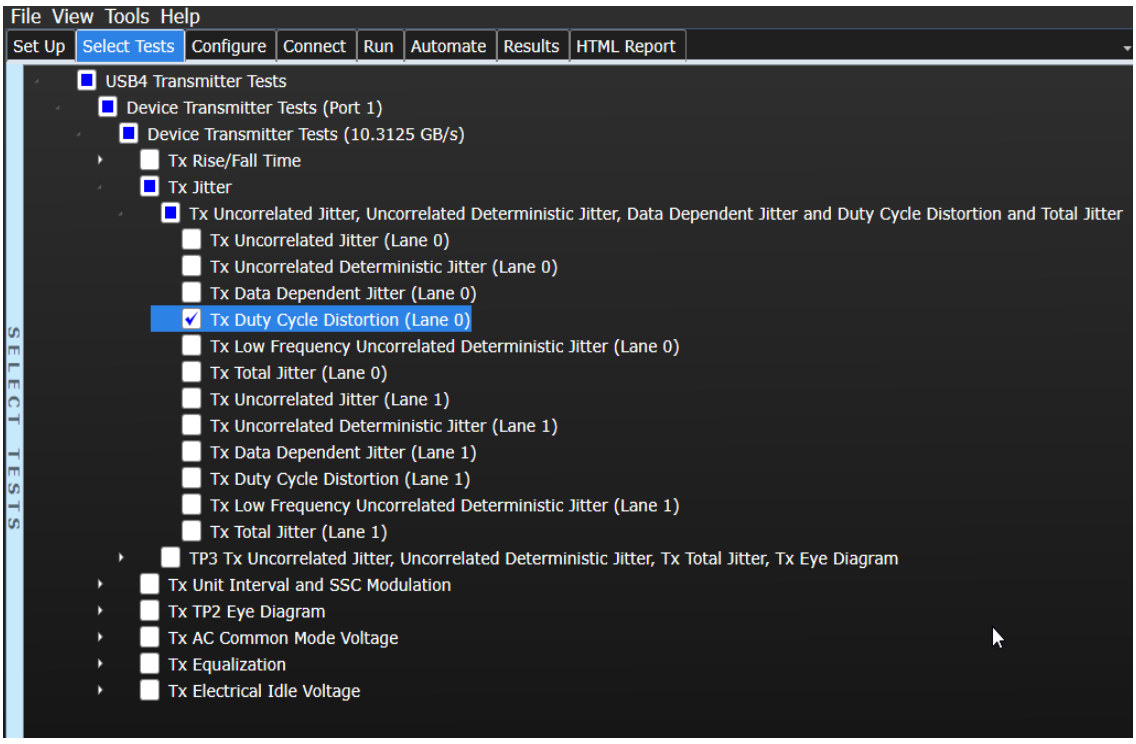


Figure 53 Selecting the Tx Duty Cycle Distortion tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2 Perform measurements with:
   a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   b Oscilloscope with a minimum bandwidth of 16GHz
3 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Pattern length – Periodic
   c Jitter Separation method must be suitable for cross-talk on the signal
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ratio to 27Mpts.
4 Capture the DCD result.
5 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If DCD > 0.03 UIp-p, the status of test is FAIL.

Test References

See

- USB4 Specification Version 2.00 (Table 3-5)

Tx Low Frequency Uncorrelated Deterministic Jitter

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Low Frequency Uncorrelated Deterministic Jitter Test is to confirm that the Low Frequency Uncorrelated Deterministic Jitter of the transmitter is within the limits of the specification.

Test Pass Requirement

Low Frequency Uncorrelated Deterministic Jitter (UDJ_LF) $\leq$ 0.04 UI_{p-p} (Refer to Table 6 on page 83).

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see Figure 41 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.
2. Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.
3. Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter, Data Dependent Jitter and Duty Cycle Distortion* are checked.

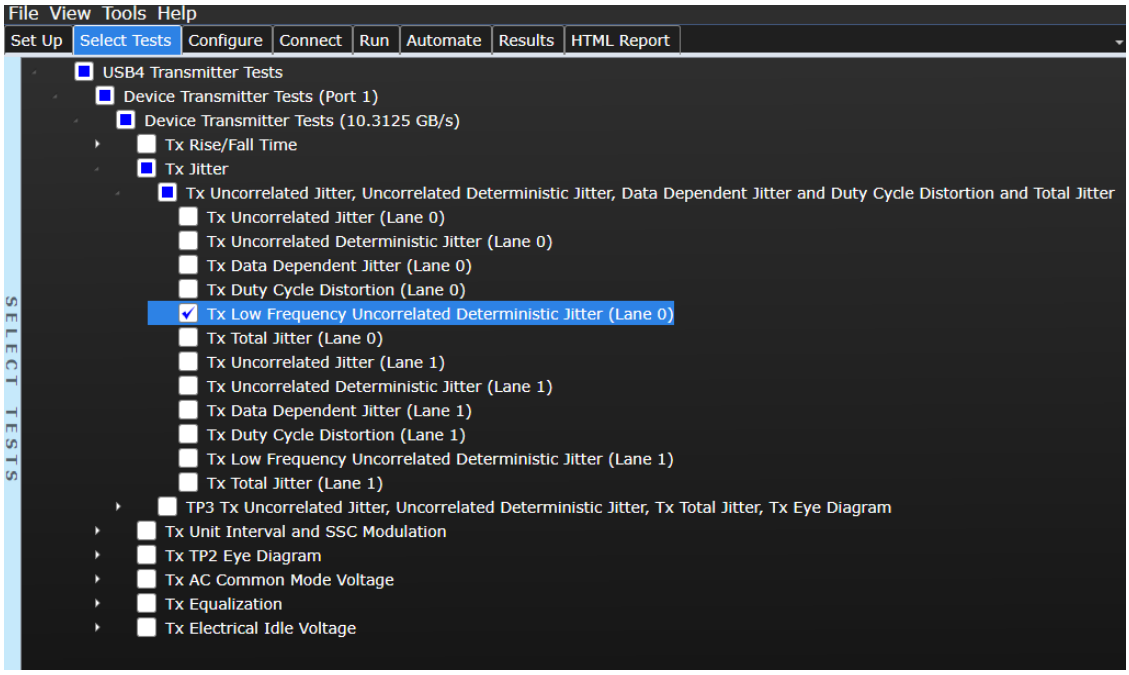


Figure 54 Selecting the Tx Low Frequency Uncorrelated Deterministic Jitter tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2 Perform measurements with:
   a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 0.5 MHz and damping factor of 0.94.
   b Apply 2^{nd} order Low-Pass-Filter with 3 dB cut-off at 2 MHz; no average and no interpolation to be used
   c Oscilloscope with a minimum bandwidth of 16GHz
3 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Pattern length – Periodic
   c Jitter Separation method must be suitable for cross-talk on the signal
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Evaluate 40 Mpts per channel when using 80 GSa/s. For higher sample rates, use memory depth in the same ratio to 40 Mpts
4 Capture the UDJ_LF result.
5 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If UDJ_LF > 0.04 UI_{p-p}, the status of test is FAIL.

Test References

See

USB4 Specification Version 2.00 (Table 3-5)

Tx Total Jitter

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Total Jitter Test is to confirm that the Total Jitter of the transmitter is within the limits of the specification.

Total Jitter (TJ) is defined as the sum of all “deterministic” components plus 14.7 times the Random Jitter (RJ) RMS. 14.7 is the factor that accommodates a Bit Error Ratio value of 1E-13.

Test Pass Requirement

Total Jitter (TJ) $\leq$ 0.38 UI_{p-p} (Refer to Table 6 on page 83).

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see Figure 41 and for configuring the USB4 Test Application, see “Setting up the USB4 Test Application" on page 48.
2. Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to “Calibration Setup for Compliance Tests" on page 56.
3. Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Total Jitter* are checked.

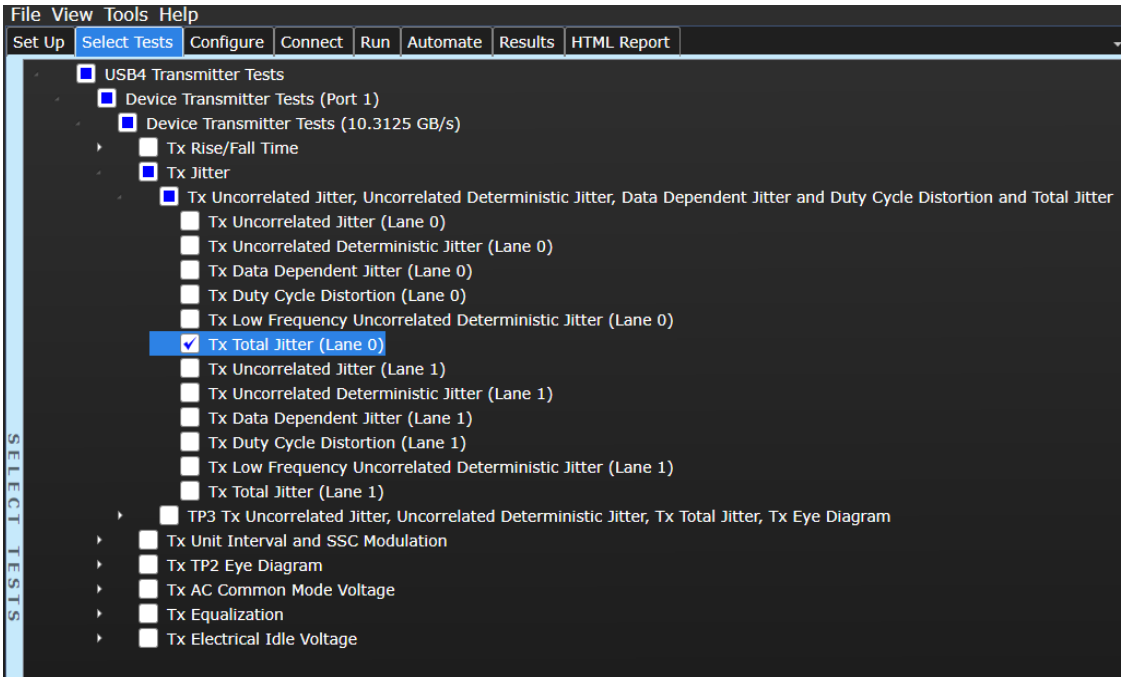


Figure 55 Selecting the Tx Total Jitter tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2 Perform measurements with:
   a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94
   b Oscilloscope with a minimum bandwidth of 16 GHz
3 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Pattern length – Periodic
   c Jitter Separation method must be suitable for cross-talk on the signal
   d Evaluate 40 Mpts per channel when using 80 GSa/s. For higher sample rates, use memory depth in the same ratio to 40 Mpts.
   e Adjust vertical scale such that the signal fits within the Oscilloscope's display.
   f Referenced to 1E-13 statistics.
4 Capture the values of Total Jitter (TJ) and Deterministic Jitter (DJ).
5 If TJ > 0.38 UI_{p-p}, perform the following steps:
   a Configure the DUT transmitter to output alternating square pattern of one 0's and one 1's on all lanes with SSC enabled. (The pattern is SQ2 instead of PRBS15).
   b Perform measurements with:
   - Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94
   - Oscilloscope with a minimum bandwidth of 16 GHz.
   c Capture the waveform and process it with the Digital Oscilloscope:
   - Sampling Rate $\geq$ 80 GSa/s
   - Pattern length – Periodic
   - Jitter Separation method must be suitable for cross-talk on the signal
   - Evaluate 40 Mpts per channel when using 80 GSa/s. For higher sample rates, use memory depth in the same ratio to 40 Mpts
   - Adjust vertical scale such that the signal fits within the Oscilloscope's display.
   - Referenced to 1E-13 statistics.
   d Capture the Random Jitter (RJ) result.
   e Calculate TJ using the equation:

$$TJ = DJ + 14.7 * RJ \text{ (DJ from \#4; PRBS15 and RJ from \#5d; SQ2)}$$

6 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If TJ > 0.38 UI_{p-p}, the status of test is FAIL.

Test References

See

USB4 Specification Version 2.00 (Table 3-5)

Tx Uncorrelated Jitter TP3

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Uncorrelated Jitter Test is to confirm that the Uncorrelated Jitter [Deterministic Jitter (DJ) and Random Jitter (RJ) components] at point TP3 of the transmitter is within the limits of the specification.

Test Pass Requirement

Uncorrelated Jitter (UJ_{TP3}) $\leq$ 0.31 UI_{p-p} (Refer to Table 7 on page 84).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 41 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter, Data Dependent Jitter and Duty Cycle Distortion* are checked.

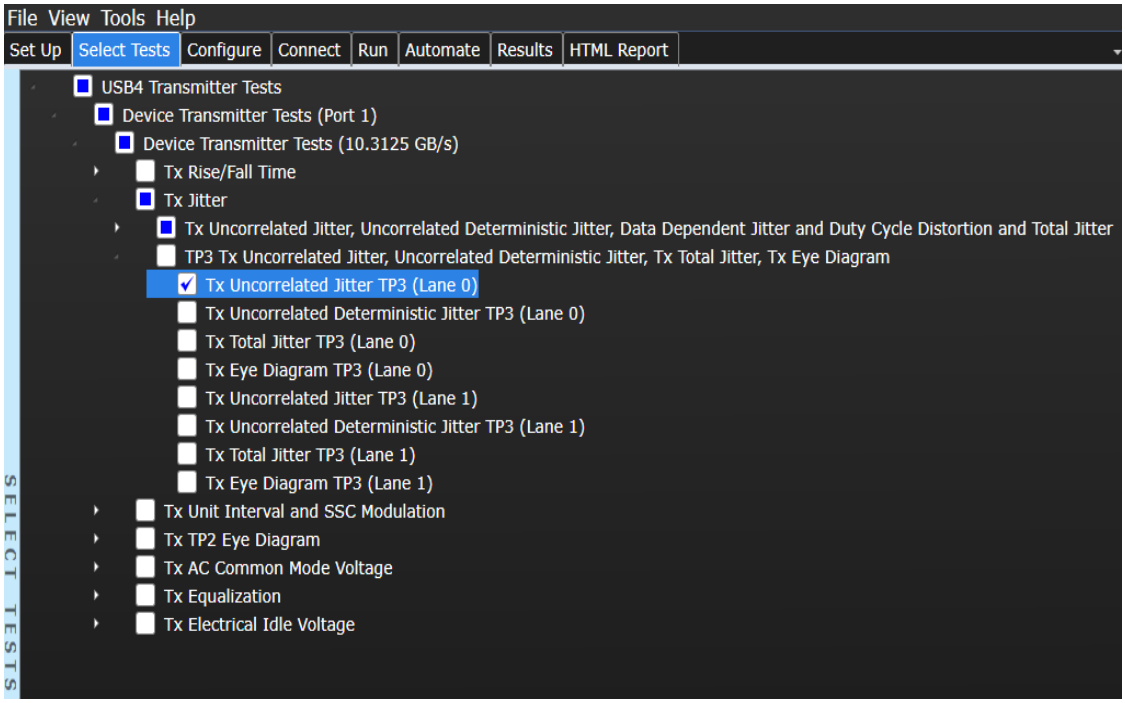


Figure 56 Selecting the Tx Uncorrelated Jitter TP3 tests

Test Procedure

1. Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2. Embed the Type-C cable in the Oscilloscope. For Gen 2 systems, use TP3_EQ embedding file *USB_2m.s4p*.
3. De-embed the cables from the test fixture to the Oscilloscope.
4. Perform measurements with:
   - *a* Reference CDR based on the 2^{nd} order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   - *b* Oscilloscope with a minimum bandwidth of 16 GHz
5. Capture the waveform and process it with the Digital Oscilloscope:
   - *a* Sampling Rate $\geq$ 80 GSa/s
   - *b* Pattern length – Periodic
   - *c* Jitter Separation method must be suitable for cross-talk on the signal
   - *d* Evaluate 40 Mpts per channel when using 80 GSa/s. For higher sample rates, use memory depth in the same ratio to 40 Mpts.
   - *e* Adjust vertical scale such that the signal fits within the Oscilloscope's display
   - *f* Referenced to 1E-13 statistics
6. Capture the values of Total Jitter (TJ_{TP3}) and Data Deterministic Jitter (DDJ_{TP3}).
7. Calculate UJ_{TP3} using the equation:

$$UJ_{TP3} = TJ_{TP3} - DDJ_{TP3}$$

8. Repeat the test for the remaining USB lanes.

Expected / Observable Results

If $UJ_{TP3} > 0.31\ UI_{p-p}$, the status of test is FAIL.

Test References

See

- *USB4 Specification Version 2.00 (Table 3-6)*

Tx Uncorrelated Deterministic Jitter TP3

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Uncorrelated Deterministic Jitter Test is to confirm that the Uncorrelated Deterministic Jitter at the point TP3 of the transmitter is within the limits of the specification.

Test Pass Requirement

Deterministic Jitter that is uncorrelated to the transmitted data (UDJ_{TP3}) $\leq$ 0.17 UI_{p-p} (Refer to Table 7 on page 84).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 41 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter, Data Dependent Jitter and Duty Cycle Distortion* are checked.

Figure 57 Selecting the Tx Uncorrelated Deterministic Jitter tests

Test Procedure

1. Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2. Embed the Type-C cable in the Oscilloscope. For Gen 2 systems, use TP3 embedding file *USB_2m.s4p*.
3. De-embed the cables from the test fixture to the Oscilloscope.
4. Perform measurements with:
   a. Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   b. Oscilloscope with a minimum bandwidth of 16GHz
5. Capture the waveform and process it with the Digital Oscilloscope:
   a. Sampling Rate $\geq$ 80 GSa/s
   b. Pattern length – Periodic
   c. Jitter Separation method must be suitable for cross-talk on the signal
   d. Evaluate 40 Mpts per channel when using 80 GSa/s. For higher sample rates, use memory depth in the same ratio to 40 Mpts
   e. Adjust vertical scale such that the signal fits within the Oscilloscope's display
6. Capture the values of Total Jitter (TJ_{TP3}) and Data Deterministic Jitter (DDJ_{TP3}).
7. Capture the UDJ_{TP3} result (same as BUJ over the Oscilloscope).
8. Repeat the test for the remaining USB lanes.

Expected / Observable Results

If $UDJ_{TP3} > 0.17\ UI_{p-p}$, the status of test is FAIL.

Test References

See

USB4 Specification Version 2.00 (Table 3-6)

Tx Total Jitter TP3

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Total Jitter TP3 Test is to confirm that the Total Jitter at point TP3 of the transmitter is within the limits of the specification.

Total Jitter (TJ) is defined as the sum of all “deterministic” components plus 14.7 times the Random Jitter (RJ) RMS. 14.7 is the factor that accommodates a Bit Error Ratio value of 1E-13.

Test Pass Requirement

Total Jitter (TJ_{TP3}) $\leq$ 0.60 UI_{p-p} (Refer to Table 7 on page 84).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 41 and for configuring the USB4 Test Application, see “Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to “Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Total Jitter* are checked.

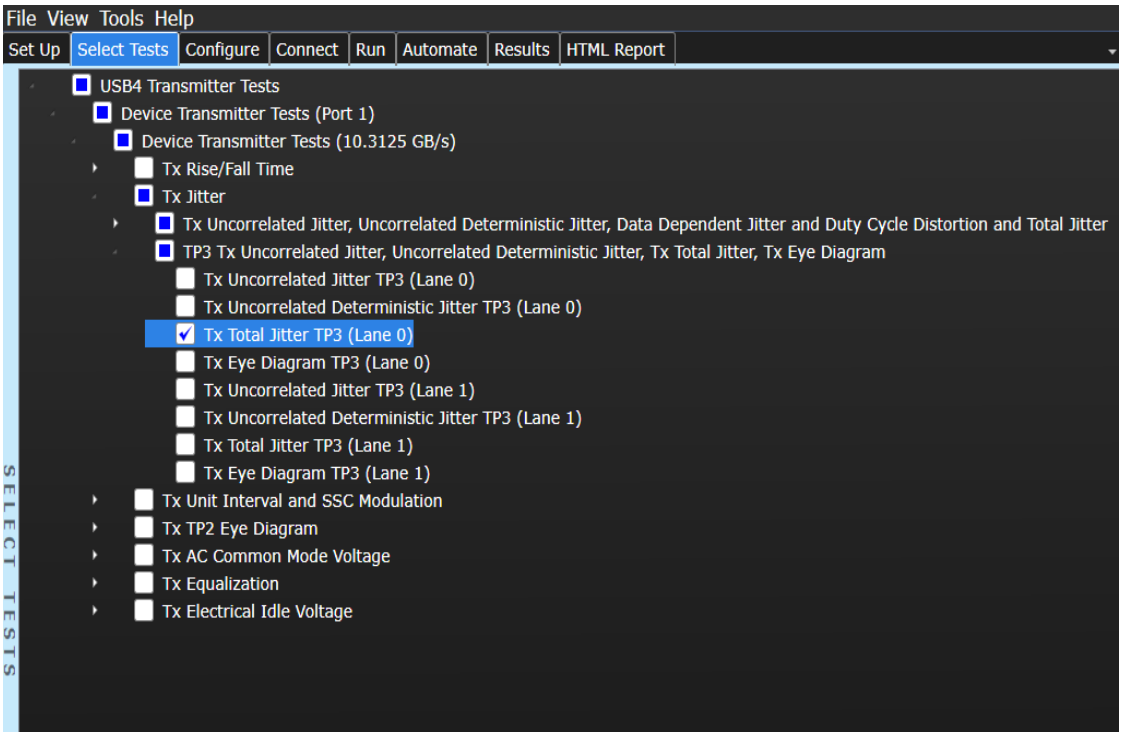


Figure 58 Selecting the Tx Total Jitter TP3 tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2 Embed the Type-C cable in the Oscilloscope. For Gen 2 systems, use TP3_EQ embedding file *USB_2m.s4p*.
3 De-embed the cables from the test fixture to the Oscilloscope.
4 Perform measurements with:
   a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   b Oscilloscope with a minimum bandwidth of 16 GHz
5 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Pattern length – Periodic
   c Jitter Separation method must be suitable for cross-talk on the signal
   d Evaluate 40 Mpts per channel when using 80 GSa/s. For higher sample rates, use memory depth in the same ratio to 40 Mpts
   e Adjust vertical scale such that the signal fits within the Oscilloscope's display
   f Referenced to 1E-13 statistics
6 Capture the values of Total Jitter (TJ_{TP3}) and Deterministic Jitter (DJ_{TP3}).
7 If $TJ_{TP3} > 0.60\ UI_{p-p}$, perform the following steps:
   a Configure the DUT transmitter to output alternating square pattern of one 0's and one 1's on all lanes with SSC enabled. (The pattern is SQ2 instead of PRBS15).
   b Perform measurements with:
   - Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94
   - Oscilloscope with a minimum bandwidth of 16 GHz

   c Capture the waveform and process it with the Digital Oscilloscope:
   - Sampling Rate $\geq$ 80 GSa/s
   - Pattern length – Periodic
   - Jitter Separation method must be suitable for cross-talk on the signal
   - Evaluate 40 Mpts per channel when using 80 GSa/s. For higher sample rates, use memory depth in the same ratio to 40 Mpts
   - Adjust vertical scale such that the signal fits within the Oscilloscope's display.
   - Referenced to 1E-13 statistics.

   d Capture the Random Jitter (RJ_{TP3}) result.
   e Calculate TJ_{TP3} using the equation:

$$TJ_{TP3} = DJ_{TP3} + 14.7 * RJ_{TP3}$$ (DJ_{TP3} from #7; PRBS15 and RJ_{TP3} from #8d; SQ2)

8 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If $TJ_{TP3} > 0.60\ UI_{p-p}$, the status of test is FAIL.

Test References

See

USB4 Specification Version 2.00 (Table 3-7)

Tx Eye Diagram TP3

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Eye Diagram TP3 Test is to confirm that the differential signal on each USB differential lane has an eye opening that meets or exceeds the limits for eye opening in the specification.

Test Pass Requirement

The eye diagram at TP3 should meet the conditions depicted in Figure 59.

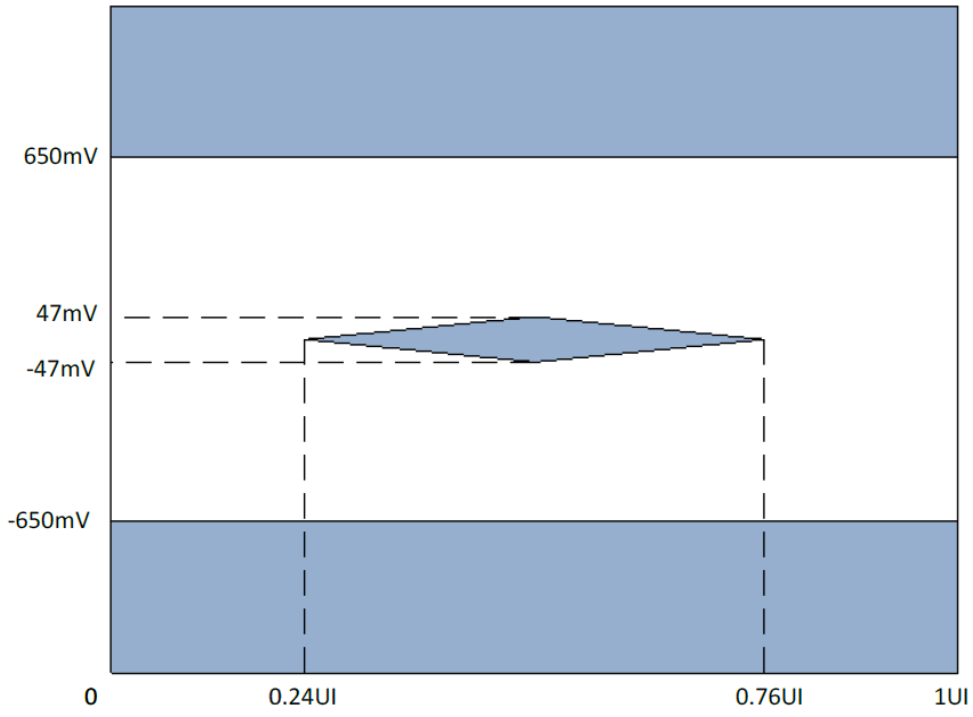


Figure 59 Pass Condition for Tx Eye Diagram TP3 Tests

(Refer to Table 7 on page 84 and Figure 59 on page 128).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter TP2/TP3 Test Setup" on page 92 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the tests under the test group *Tx Eye Diagram* are checked.

Figure 60 Selecting the Tx Eye Diagram TP3 tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2 Embed the Type-C cable in the Oscilloscope. For Gen 2 systems, use TP3_EQ embedding file *USB_2m.s4p*.
3 De-embed the cables from the test fixture to the Oscilloscope.
4 Perform measurements with:
   a Change from no interpolation to X16 a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and X16 interpolation to be used.
   b Oscilloscope with a minimum bandwidth of 16GHz
5 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Adjust vertical and horizontal scale such that the signal fits within the Oscilloscope's display
   c Accumulate at 1E6 UI
6 Compare the data eye to the TP3 eye diagram mask. Check for conditions described in the section "Expected / Observable Results".
7 Repeat the test for the remaining USB lanes.

Expected / Observable Results

i If any part of the waveform exceeds either the inner or outer eye height voltage (+/-1000mV), the status of the test is FAIL.
ii If any part of the waveform hits the mask, the status of the test is FAIL.

Test References

See

USB4 Specification Version 2.00 (Table 3-6)

Tx Average Unit Interval, Min/Max

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Average Unit Interval Test is to confirm that the mean unit interval at TP1 of a USB4 device, under all conditions, does not exceed the minimum or maximum limits of the specification. The average UI should be measured over windows at the size of one SSC cycle.

Test Pass Requirement

Average Unit Interval, Min

97.1348 ps <= Average Unit Interval, Min (Device, 10.3125 Gb/s) <= 97.2420 ps

Average Unit Interval, Max

97.1348 ps <= Average Unit Interval, Max (Device, 10.3125 Gb/s)<= 97.2420 ps

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see Figure 41 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.
2. Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.
3. Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Unit Interval and SSC Down Spread Modulation* are checked.

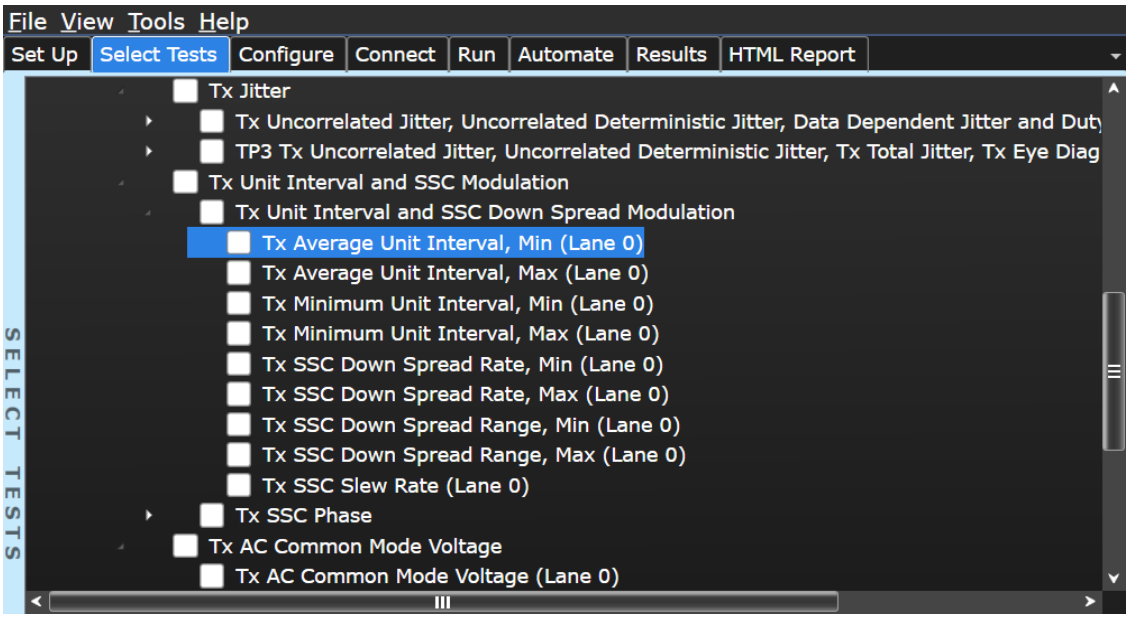


Figure 61 Selecting the Tx Unit Interval tests

Test Procedure

1. Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2. Capture the waveform and process it with the Digital Oscilloscope:
   - *a* Sampling Rate $\geq$ 80 GSa/s
   - *b* Evaluate 27 Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ratio to 27Mpts
   - *c* No CDR, no average and no interpolation to be used
   - *d* Adjust vertical scale such that the signal fits within the Oscilloscope's display
   - *e* Oscilloscope must have a minimum bandwidth of 16GHz
3. Calculate UI dynamically using a uniform moving average filter procedure with a window size of 3000 symbols.
4. Measure the values of both UI_{MAX} and UI_{MIN}.
5. Repeat the test for the remaining USB lanes.

Expected / Observable Results

The status of the test is fail if.

Average Unit Interval, Min

97.1348 ps >= Average Unit Interval, Min (Device, 10.3125 Gb/s) >= 97.2420 ps

Average Unit Interval, Max

97.1348 ps >= Average Unit Interval, Max (Device, 10.3125 Gb/s) >= 97.2420 ps

Test References

See

- *USB4 Specification Version 2.00*

Tx Minimum Unit Interval, Min/Max

Test Overview

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

The objective of the Tx Unit Interval Test is to confirm that the data rate, under all conditions, does not exceed the minimum or maximum limits of the specification.

Test Pass Requirement

G2_UI_MIN ≤ Unit Interval ≤ G2_UI_MAX (Refer to Table 6 on page 83).

G2_UI_MIN ≥ 96.9406 ps

G2_UI_MAX ≤ 96.9988 ps

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 41 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Unit Interval and SSC Down Spread Modulation* are checked.

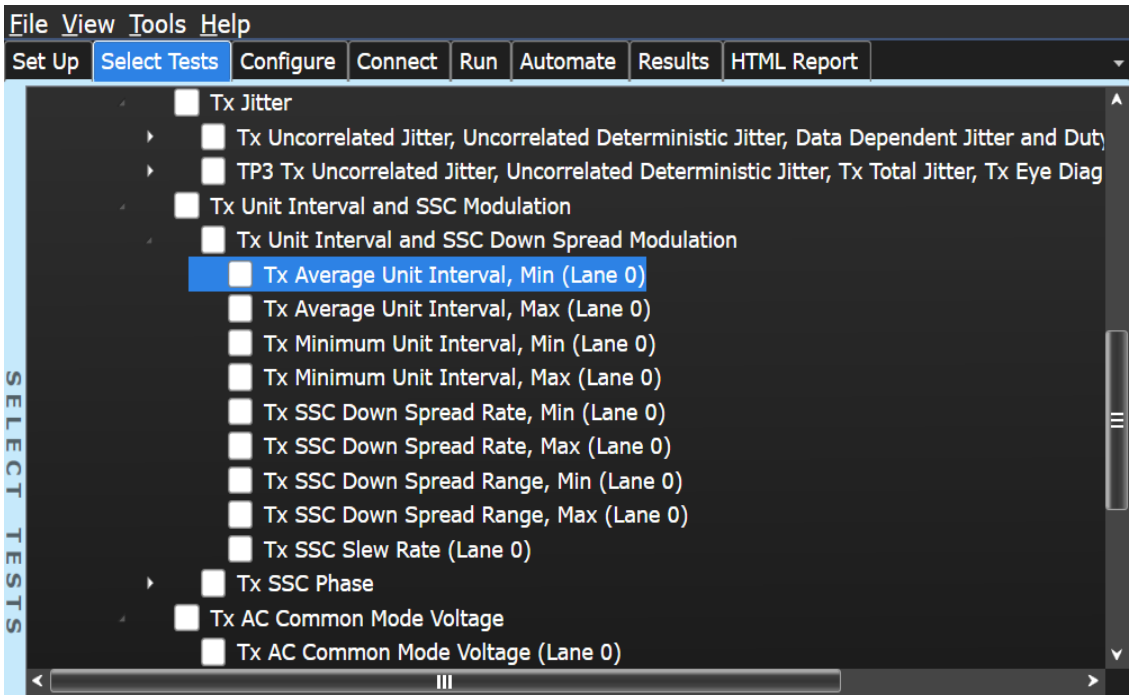


Figure 62 Selecting the Tx Unit Interval tests

Test Procedure

1. Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2. Capture the waveform and process it with the Digital Oscilloscope:
   - *a* Sampling Rate $\geq$ 80 GSa/s
   - *b* Evaluate 27 Mpts per channel when using 80 GSa/s. For higher sample rates, use memory depth in the same ratio to 27 Mpts
   - *c* No CDR, no average and no interpolation to be used
   - *d* Adjust vertical scale such that the signal fits within the Oscilloscope's display
   - *e* Oscilloscope must have a minimum bandwidth of 16 GHz
3. Calculate UI dynamically using a uniform moving average filter procedure with a window size of 3000 symbols.
4. Measure the values of both UI_{MAX} and UI_{MIN}.
5. Repeat the test for the remaining USB lanes.

Expected / Observable Results

If UI_{MAX} > G2_UI_MAX, the status of test is FAIL.

If UI_{MIN} < G2_UI_MIN, the status of test is FAIL.

Test References

See

- *USB4 Specification Version 2.00 (Table 13-1)*

Tx SSC Down Spread Rate

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx SSC Down Spread Rate Test is to confirm that the Link clock down-spreading modulation rate is within the limits of the specification.

Test Pass Requirement

SSC_DSR_MIN $\leq$ SSC_Down_Spread_Rate $\leq$ SSC_DSR_MAX (Refer to Table 3 on page 74).

SSC_DSR_MAX $\leq$ 37.00 kHz

SSC_DSR_MIN $\geq$ 35.00 kHz

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 41 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Unit Interval and SSC Down Spread Modulation* are checked.

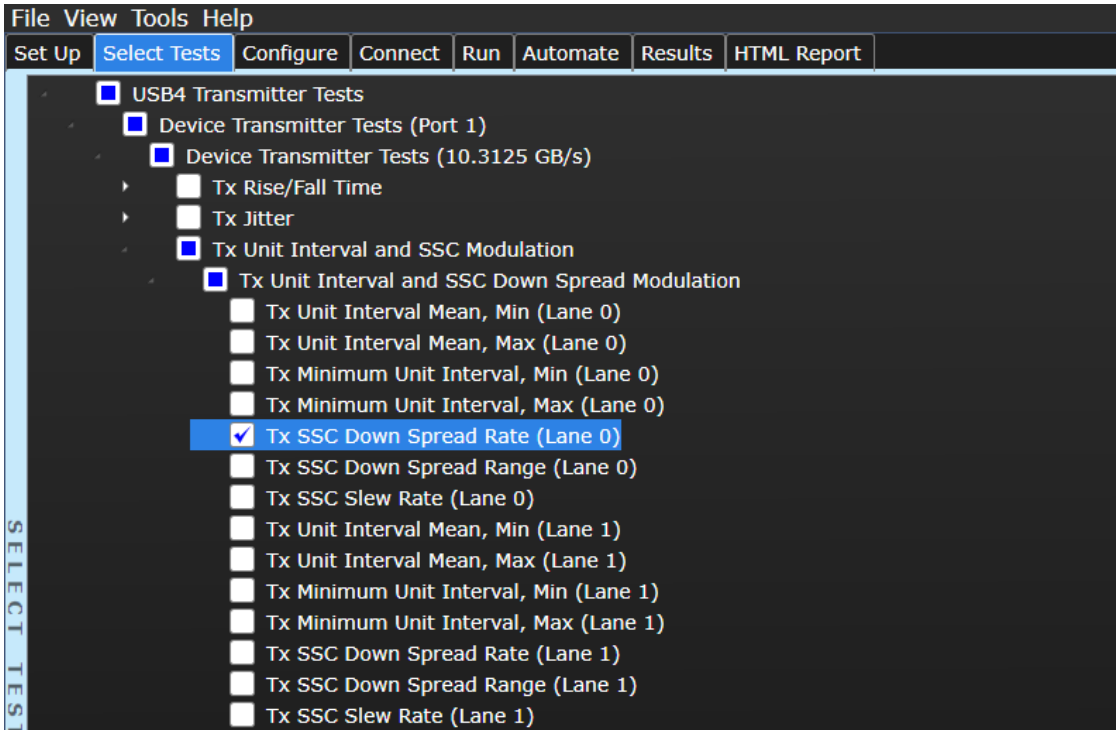


Figure 63 Selecting the Tx SSC Down Spread Rate tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ratio to 27Mpts
   c No CDR, no average and no interpolation to be used
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Oscilloscope must have a minimum bandwidth of 16GHz
3 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If SSC_DSR_MIN > SSC_Down_Spread_Rate > SSC_DSR_MAX, the status of test is FAIL.

Test References

See

- *USB4 Specification Version 2.00 (Table 13-1)*

Tx SSC Down Spread Range

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx SSC Down Spread Range Test is to confirm that the data down spreading is within the limits of the specification.

Test Pass Requirement

0.4 % ≤ SSC_Down_Spread_Range ≤ 0.5 % (Refer to Table 3 on page 74).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 41 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Unit Interval and SSC Down Spread Modulation* are checked.

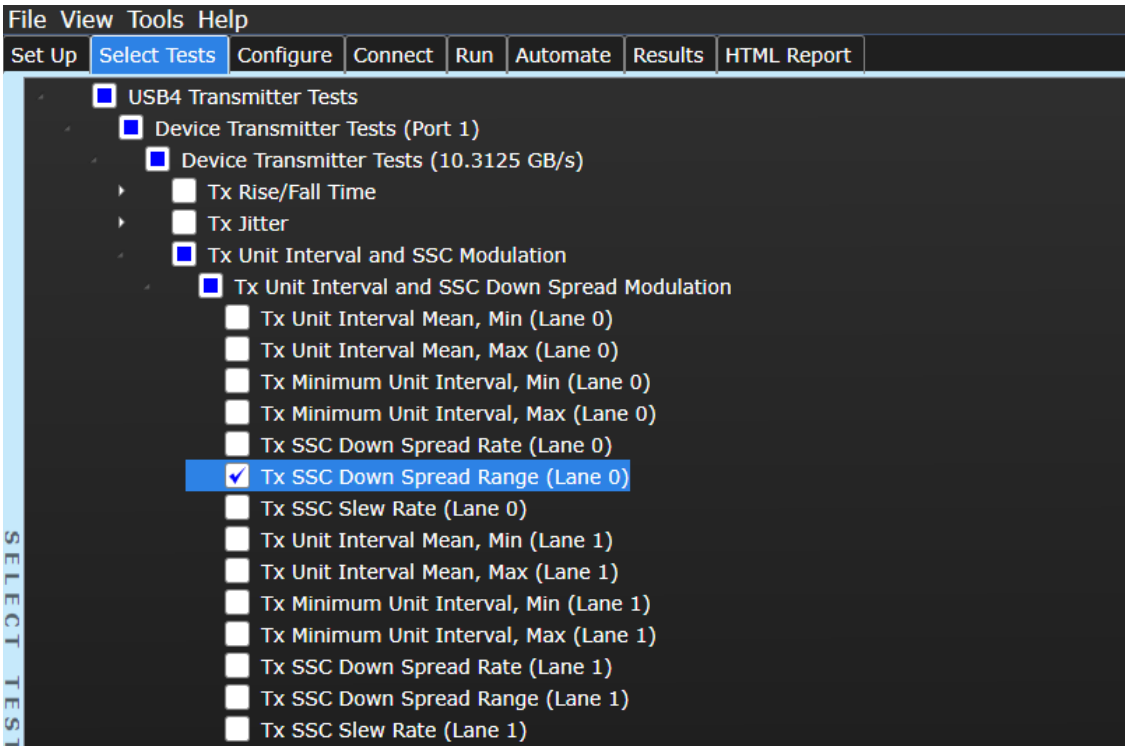


Figure 64 Selecting the Tx SSC Down Spread Range tests

Test Procedure

1. Run the "Tx Eye Diagram TP3" Test as a prerequisite to obtain UI_{MAX} and UI_{MIN}.
2. Use the obtained value of UI_{MAX} and UI_{MIN} to calculate the Range percentage:

$$\text{Maximum Deviation} = 100*\{[10.3125G - (1 / UI_{MAX})] / 10.3125G\}$$

$$\text{Minimum Deviation} = 100*\{[10.3125G - (1 / UI_{MIN})] / 10.3125G\}$$

3. Calculate SSC Down Spread Range using the equation:

$$\text{Maximum Deviation - Minimum Deviation}$$

4. Repeat the test for all remaining USB lanes.

Expected / Observable Results

If SSC_Down_Spread_Range > 0.5% or SSC_Down_Spread_Range < 0.4%, the status of test is FAIL.

Test References

See

USB4 Specification Version 2.00 (Table 3-2)

Tx SSC Slew Rate

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx SSC Slew Rate Test is to confirm that the SSC Slew Rate is within the limits of the specification.

Test Pass Requirement

SSC_Slew_Rate $\leq$ 1.2500 kppm/us (Refer to Table 3 on page 74).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 41 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Unit Interval and SSC Down Spread Modulation* are checked.

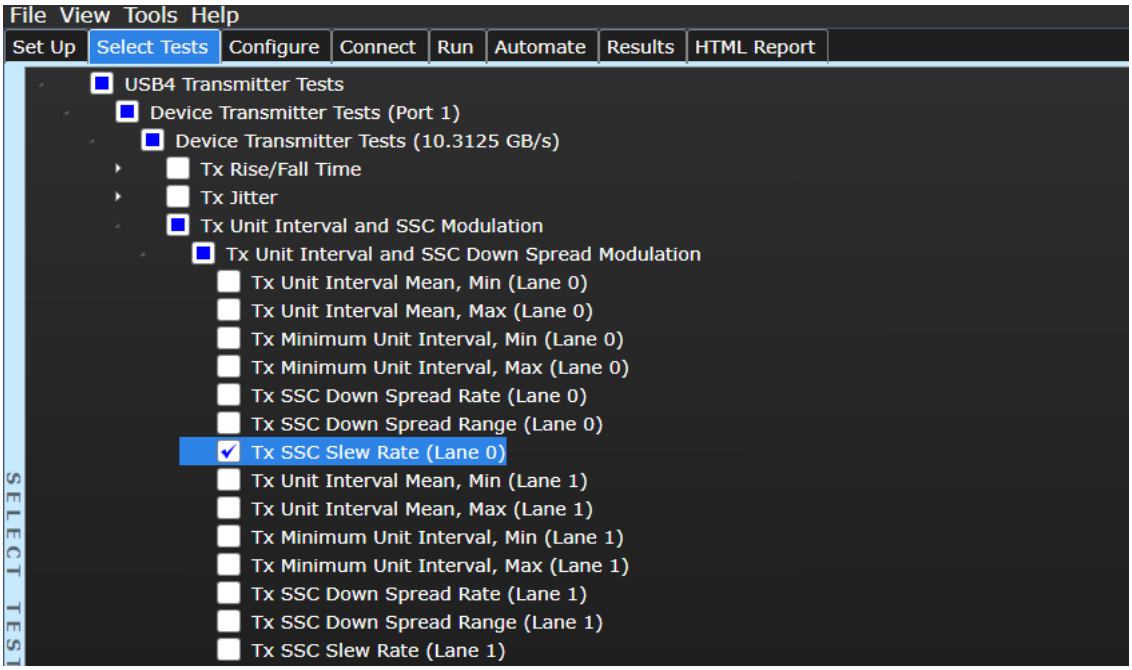


Figure 65 Selecting the Tx SSC Slew Rate tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2 Capture the waveform and post process it with an appropriate software:
   a Sampling Rate $\geq$ 80 GSa/s
   b Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ratio to 27Mpts
   c No CDR, no average and no interpolation to be used
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Extract SSC slew rate from the transmitted signal over measurement intervals of 0.5µs
   f Extract SSC slew rate from the phase information after applying a 2^{nd} order Low-Pass-Filter with 3 dB cut-off at 5 MHz.
   g Oscilloscope must have a minimum bandwidth of 16 GHz
3 SSC_Slew_Rate is measured as the SSC frequency deviation over time while valid data is being transmitted in which 1E-12 bit error rate is required without assuming forward error correction.
4 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If SSC_Slew_Rate > 1.2500 kppm/us, the status of test is FAIL.

Test References

See

USB4 Specification Version 2.00 (Table 3-2)

Tx SSC Phase Deviation

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx SSC Phase Deviation Test is to confirm that the SSC Phase Deviation is within the limits of the specification.

Test Pass Requirement

2.5 ns p-p $\leq$ SSC_Phase_Deviation $\leq$ 22.0 ns p-p (Refer to Table 3 on page 74).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 41 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx SSC Phase* are checked.

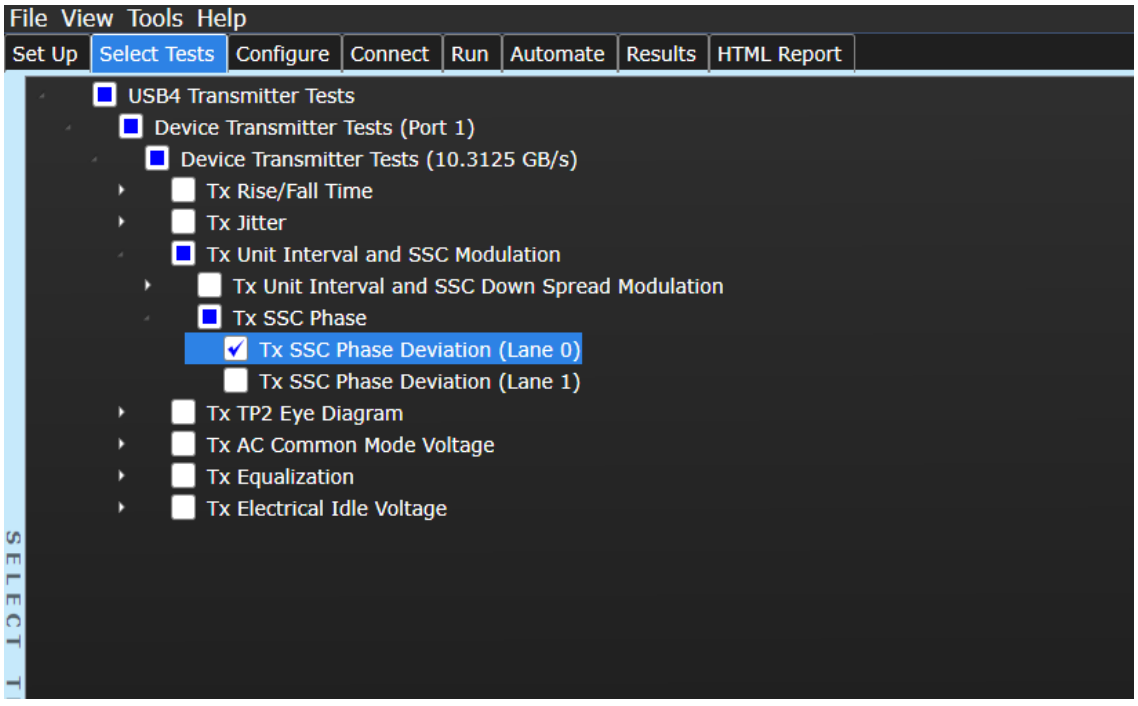


Figure 66 Selecting the Tx SSC Phase Deviation tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2 Capture the waveform and process it with the Digital Oscilloscope's software:
   a Sampling Rate $\geq$ 80 GSa/s
   b Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ratio to 27 Mpts
   c No CDR, no average and no interpolation to be used
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Oscilloscope must have a minimum bandwidth of 16 GHz
3 Extract the SSC Phase Deviation from the transmitted signal.
4 Extract the SSC Phase Deviation from the phase jitter after applying a 2^{nd} order low-pass filter with 3dB point at 5 MHz.
5 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If 2.5 ns p-p > SSC_Phase_Deviation > 22.000 ns p-p the status of test is FAIL.

Test References

See

- *USB4 Specification Version 2.00 (Table 13-1)*

Tx Eye Diagram

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Eye Diagram Test is to confirm that the differential signal on each USB differential lane has an eye opening that meets or exceeds the limits for eye opening in the specification.

Test Pass Requirement

The eye diagram should meet the conditions depicted in Figure 67.

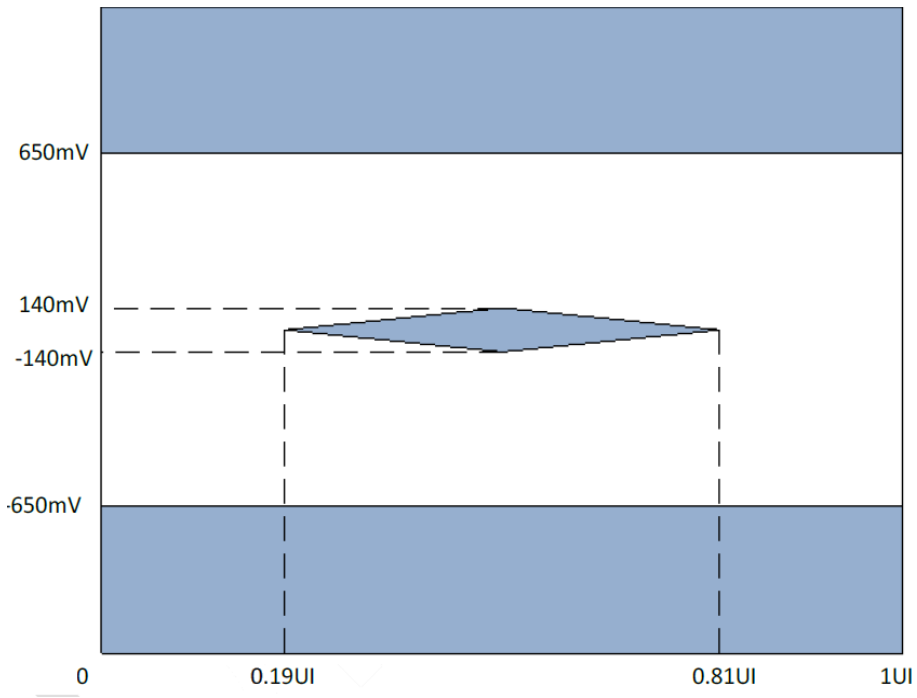


Figure 67 Pass Condition for Tx Eye Diagram Tests

(Refer to Table 6 on page 83 and Figure 67 on page 143)

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter TP2/TP3 Test Setup" on page 92 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Eye Diagram* are checked.

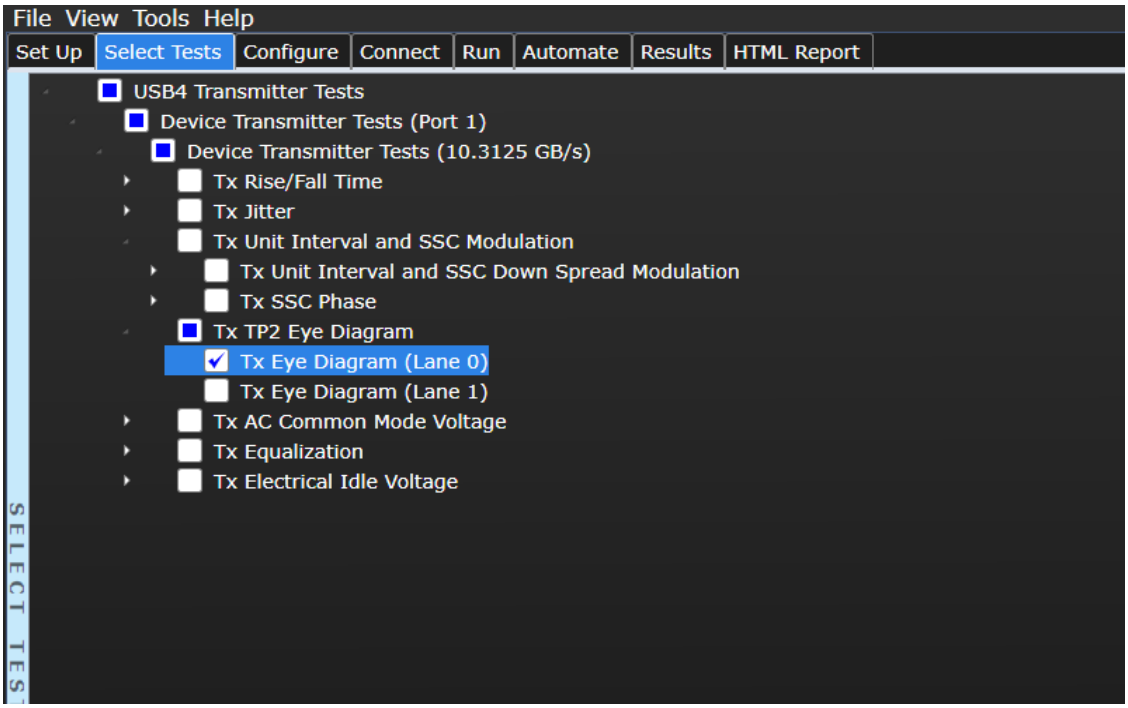


Figure 68 Selecting the Tx Eye Diagram tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.

2 Perform measurements with:

a Change from no interpolation to X16 a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and X16 interpolation to be used.

b Oscilloscope with a minimum bandwidth of 16GHz

3 Capture the waveform and process it with the Digital Oscilloscope:

a Sampling Rate $\geq$ 80 GSa/s

b Adjust vertical scale such that the signal fits within the Oscilloscope's display

c Measured at 1E6 UI

4 Compare the data eye to the TP1 eye diagram mask. Check for conditions described in the section "Expected / Observable Results".

5 Perform measurements with: Repeat the test for the remaining USB lanes.

Expected / Observable Results

i If any part of the waveform exceeds either the inner or outer height voltage (+/- 700mV), the status of the test is FAIL.

ii If any part of the waveform hits the mask, the status of the test is FAIL.

Test References

See

- USB4 Specification Version 2.00(Table 3-5)

Tx AC Common Mode Voltage

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx AC Common Mode Voltage Test is to confirm that the transmitter common mode on the USB differential signals is within the limits of the specification.

Test Pass Requirement

TX AC Common Mode Voltage $\leq$ 100 mV_{p-p} (Refer to Table 6 on page 83).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 41 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the tests under the test group *Tx AC Common Mode Voltage* are checked.

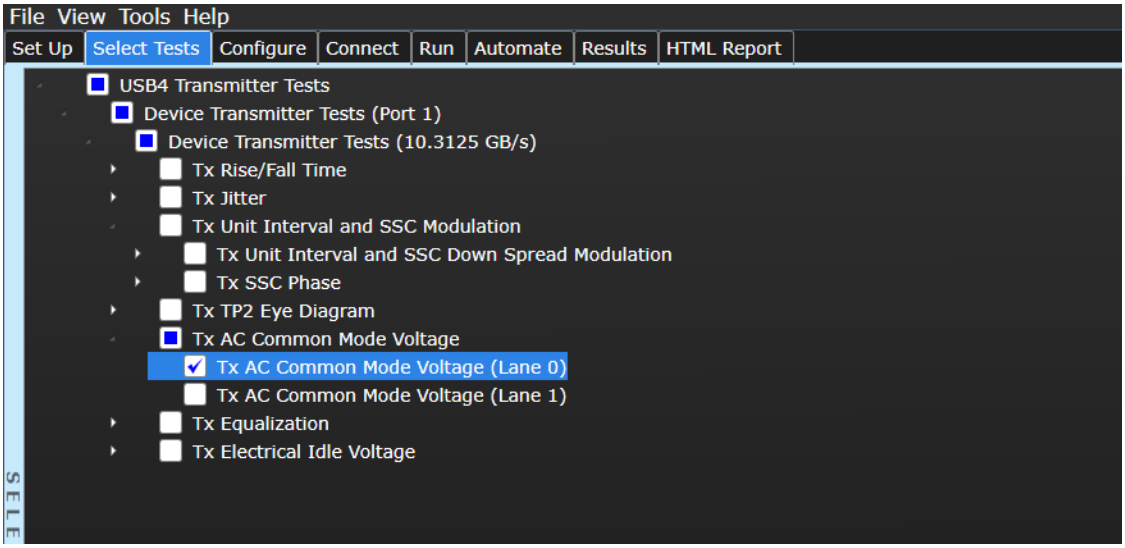


Figure 69 Selecting the Tx AC Common Mode Voltage tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Evaluate 27 Mpts per channel when using 80 GSa/s. For higher sample rates, use memory depth in the same ratio to 27 Mpts
   c No CDR, no average and no interpolation to be used
   d Oscilloscope must have a minimum bandwidth of 16 GHz
3 Calculate the AC Common Mode Voltage (V_{AC-CM}) using the equation:

$$V_{AC-CM} = (V_{TX-P} + V_{TX-N}) / 2$$

4 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If $V_{AC-CM} > 100\ mV_{p-p}$, the status of test is FAIL.

Test References

See

USB4 Specification Version 2.00 (Table 3-5)

Tx Equalization Tests

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Equalization Tests is to confirm that the transmitter equalization is within the limits of the specification. The Tx Equalization Tests are further divided into three tests, namely:

- Tx Equalization Preshoot
- Tx Equalization Deemphasis
- Tx Swing Preset 15

Test Pass Requirement

Transmitter Swing: 3.5 ± 1dB (for preset 15 only)

Preshoot, De-Emphasis: ± 1dB for the following presets:

Table 10 Transmitter Equalization Presets

Preset Number	Pre-Shoot	De-Emphasis	Informative Filter Coefficients		
			C_{-1}	C_0	C_1
0	0	0	0	1	0
1	0	-1.9	0	0.90	-0.10
2	0	-3.6	0	0.83	-0.17
3	0	-5.0	0	0.78	-0.22
4	0	-8.4	0	0.69	-0.31
5	0.9	0	-0.05	0.95	0
6	1.1	-1.9	-0.05	0.86	-0.09
7	1.4	-3.8	-0.05	0.79	-0.16
8	1.7	-5.8	-0.05	0.73	-0.22
9	2.1	-8.0	-0.05	0.68	-0.27
10	1.7	0	-0.09	0.91	0
11	2.2	-2.2	-0.09	0.82	-0.09
12	2.5	-3.6	-0.09	0.77	-0.14
13	3.4	-6.7	-0.09	0.69	-0.22
14	3.6	0	-0.17	0.83	0
15	1.7	-1.7	-0.05	0.55	-0.05

(Refer to Table 5 on page 81).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 41 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the tests under the test group *Tx Equalization* are checked.

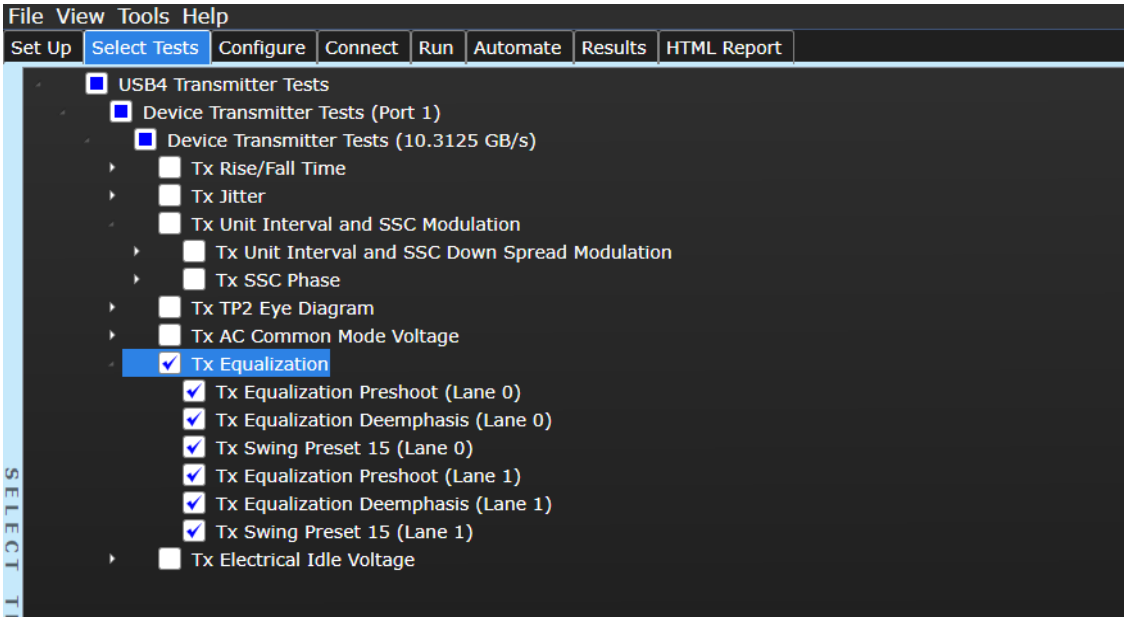


Figure 70 Selecting the Tx Equalization Tests

4 Under the **Configure** tab of the Test Application, select **ALL** for the Configuration Variable “Tx Equalization” to run the tests for preset numbers P0 to P15.

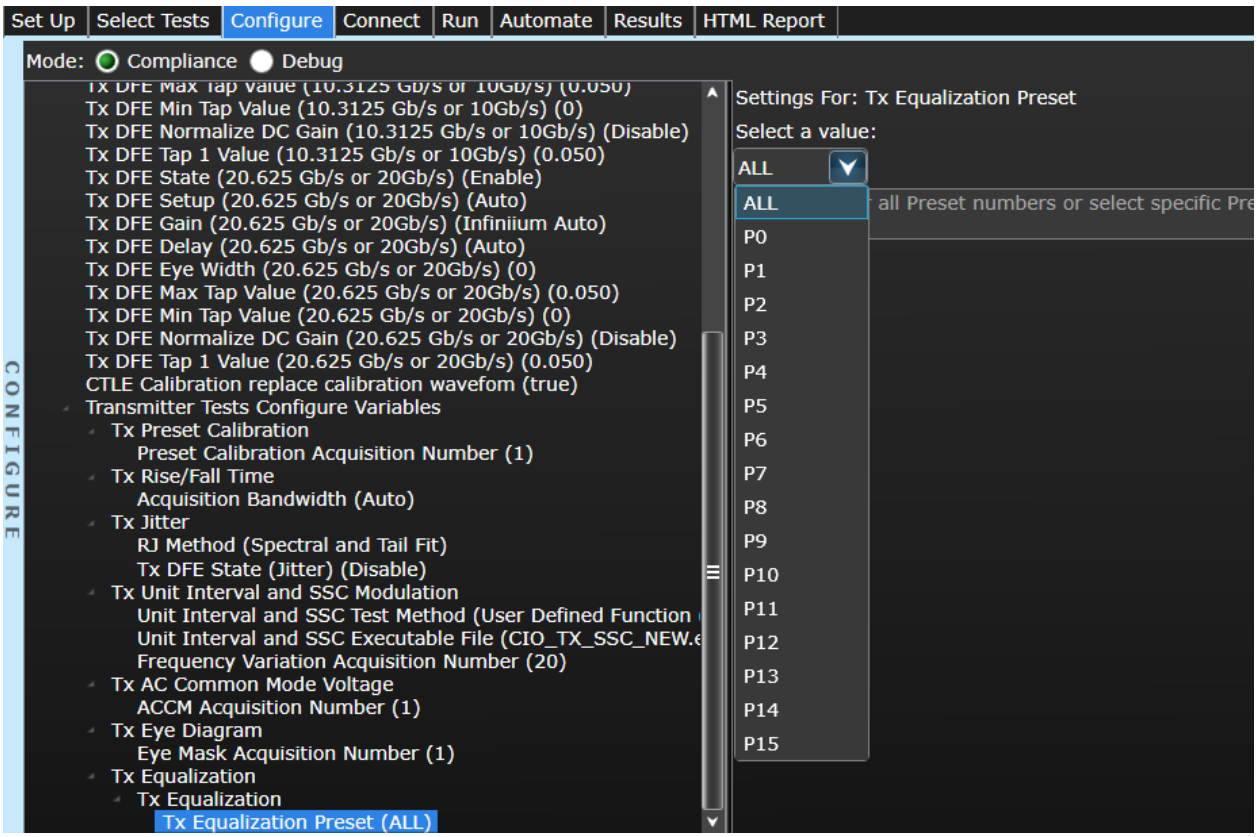


Figure 71 Configuring Tx Equalization Preset Variable

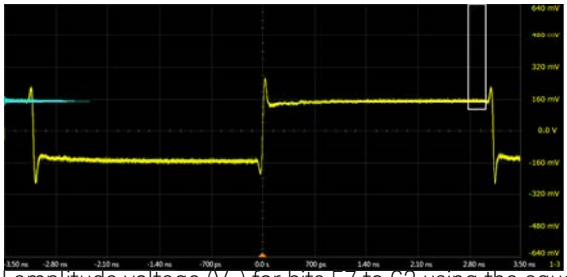
Test Procedure

1 Set Preset 0 (P0).

2 Configure the DUT transmitter to output alternating square pattern of 64 0's and 64 1's on all lanes with SSC enabled along with both pre-shoot and de-emphasis enabled.

3 Adjust vertical scale such that the signal fits within the Oscilloscope's display.

4 Average one cycle using 150 cycles; no CDR and no interpolation to be used. Oscilloscope must have a minimum bandwidth of 16 GHz.



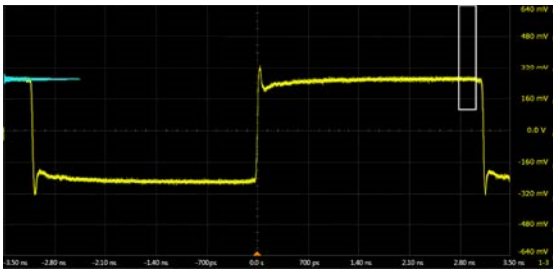
5 Measure differential amplitude voltage (V_1) for bits 57 to 62 using the equation:

$$V_1 = [|V_{bits(57\text{-}62)} \text{ (64 bits of 1's)} - V_{bits(57\text{-}62)} \text{ (64 bits of 0's)}|]$$

6 Configure the DUT transmitter to output alternating square pattern of 64 0's and 64 1's on all lanes with SSC enabled along with de-emphasis enabled but no pre-shoot.

7 Adjust vertical scale such that the signal fits within the Oscilloscope's display.

8 Average one cycle using 150 cycles; no CDR and no interpolation to be used. Oscilloscope must have a minimum bandwidth of 16 GHz.



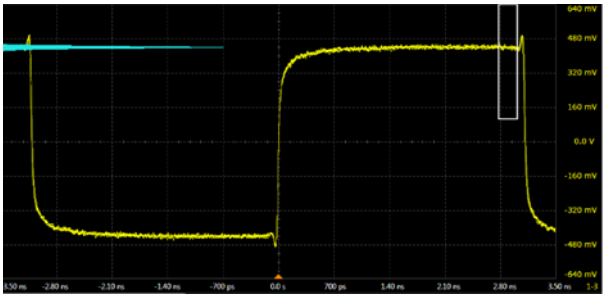
9 Measure differential amplitude voltage (V_2) for bits 57 to 62 using the equation:

$$V_2 = [|V_{bits(57\text{-}62)} \text{ (64 bits of 1's)} - V_{bits(57\text{-}62)} \text{ (64 bits of 0's)}|]$$

10 Configure the DUT transmitter to output alternating square pattern of 64 0's and 64 1's on all lanes with SSC enabled along with pre-shoot enabled but no de-emphasis.

11 Adjust vertical scale such that the signal fits within the Oscilloscope's display.

12 Average one cycle using 150 cycles; no CDR and no interpolation to be used. Oscilloscope must have a minimum bandwidth of 16GHz.



13 Measure differential amplitude voltage (V_3) for bits 57 to 62 using the equation:

$$V_3 = [|V_{bits(57\text{-}62)} \text{ (64 bits of 1's)} - V_{bits(57\text{-}62)} \text{ (64 bits of 0's)}|]$$

Set Pre-Shoot to be $20 * \log_{10} [V_2/V_1]$

Set De-Emphasis to be $20 * \log_{10} [V_1/V_3]$

14 Repeat steps 2 to 10 for all Presets defined in Table 10.

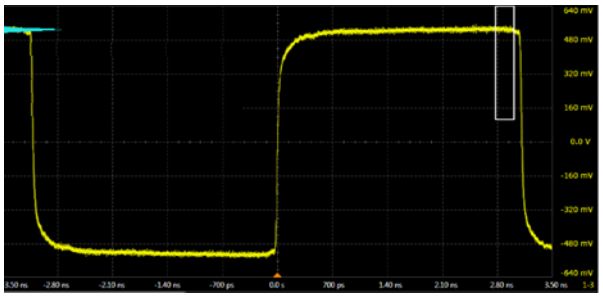
15 Check for PASS/FAIL conditions for both Pre-shoot and De-emphasis.

16 Set the DUT to Preset 0 (P0).

17 Configure the DUT transmitter to output alternating square pattern of 64 0's and 64 1's on all lanes with SSC enabled but with both pre-shoot and de-emphasis disabled.

18 Adjust vertical scale such that the signal fits within the Oscilloscope's display.

19 Average one cycle using 150 cycles; no CDR and no interpolation to be used. Oscilloscope must have a minimum bandwidth of 16GHz.



20 Measure differential amplitude voltage (V_0) for bits 57 to 62 using the equation:

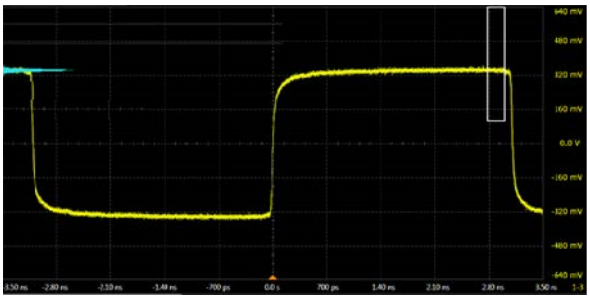
$$V_0 = [|V_{bits(57\text{-}62)} \text{ (64 bits of 1's)} - V_{bits(57\text{-}62)} \text{ (64 bits of 0's)}|]$$

21 Set the DUT to Preset 15 (P15).

22 Configure the DUT transmitter to output alternating square pattern of 64 0's and 64 1's on all lanes with SSC enabled but with both pre-shoot and de-emphasis disabled.

23 Adjust vertical scale such that the signal fits within the Oscilloscope's display

24 Average one cycle using 150 cycles; no CDR and no interpolation to be used. Oscilloscope must have a minimum bandwidth of 16GHz.



25 Measure differential amplitude voltage (V_{15}) for bits 57 to 62 using the equation:

$$V_{15} = [|V_{bits(57\text{-}62)} \text{ (64 bits of 1's)} - V_{bits(57\text{-}62)} \text{ (64 bits of 0's)}|]$$

$$\text{Set Swing to be } 20 * \log_{10} [V_0/V_{15}]$$

26 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If the Preshoot for a particular Preset number is not within ± 1dB of the matching value in Table 10, the status of test is FAIL.

If the De-Emphasis for a particular Preset number is not within ± 1dB of the matching value in Table 10, the status of test is FAIL.

If Swing < 2.5 dB or Swing > 4.5 dB, the status of test is FAIL.

Test References

See

- *USB4 Specification Version 2.0 (Table 3-4)*

Tx Electrical Idle Voltage Test

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Electrical Idle Voltage Test is to confirm that the transmitter peak voltage during electrical idle do not exceed the limits of the specification.

Test Pass Requirement

Tx Electrical Idle Voltage ≤ 20 mV_{p-p}

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 41 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the tests under the test group **Tx Electrical Idle Voltage** are selected.

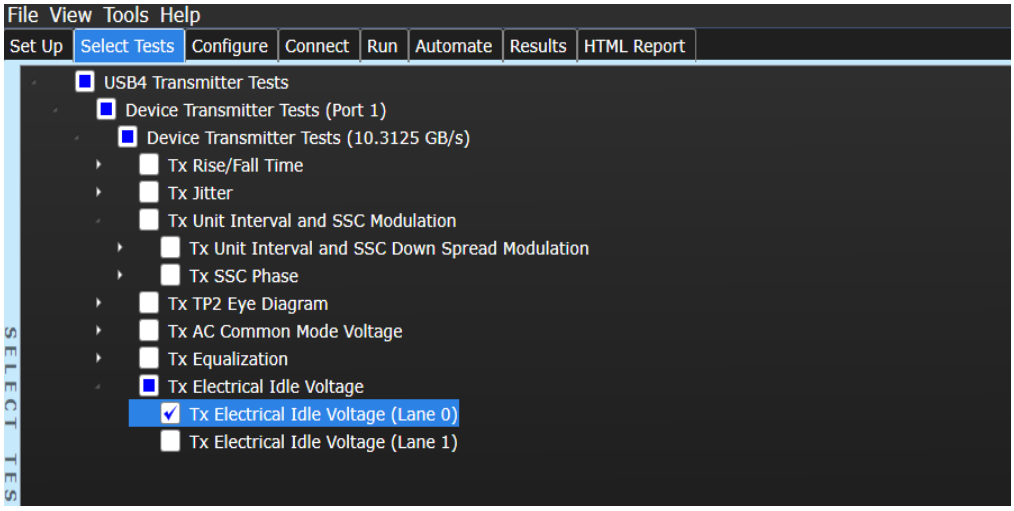


Figure 72 Selecting the Tx Electrical Idle Voltage Tests

Test Procedure

1 Configure the DUT to be in electrical idle mode.
2 Capture the waveform, and process it with the Digital Oscilloscope.
   a Sampling Rate ≥ 80 GSa/s.
   b Evaluate 10 Mpts per channel when using 80 GSa/s. For higher sampling rate, use memory depth in the same ratio to 10 Mpts.
   c No CDR, no average, and no interpolation to be used.
   d Oscilloscope must have a minimum bandwidth of 16 GHz (Gen 2) 21 GHz (Gen 3).
3 Calculate the TX Electrical Idle Voltage (V_ELEC_IDLE) using this equation:
   $V_{PEAK} = V_{TX-P} - V_{TX-N}$
4 $V_{\_ELEC\_IDLE}$ shall be extracted after applying first order low-pass filter with 3 dB point at 1.25 GHz.
5 Repeat the test for the remaining USB4 lanes.

Measurement Procedure

1 Verify the input signal.
   a Verify the input signal's amplitude.
   b Scale the vertical display of the input signal to optimum value.
2 Capture the input signal, and create the differential signal.
3 Setup the parameter of the general measurement.
   a Enable measure all edges to obtain the statistical values of the measurement.
4 Setup the following measurement:
   a Peak-to-peak voltage (V_{pp})
   b Root-mean-square voltage (V_{rms})
5 Report the Electrical Idle Output Voltage measurement results.

Expected / Observable Results

V_ELEC_IDLE > 20 mV_{p-p}, the status of test is FAIL

Test References

See

- *USB4 Specification Version 2.00 (Table 3-2)*

Tx Differential Return Loss Test

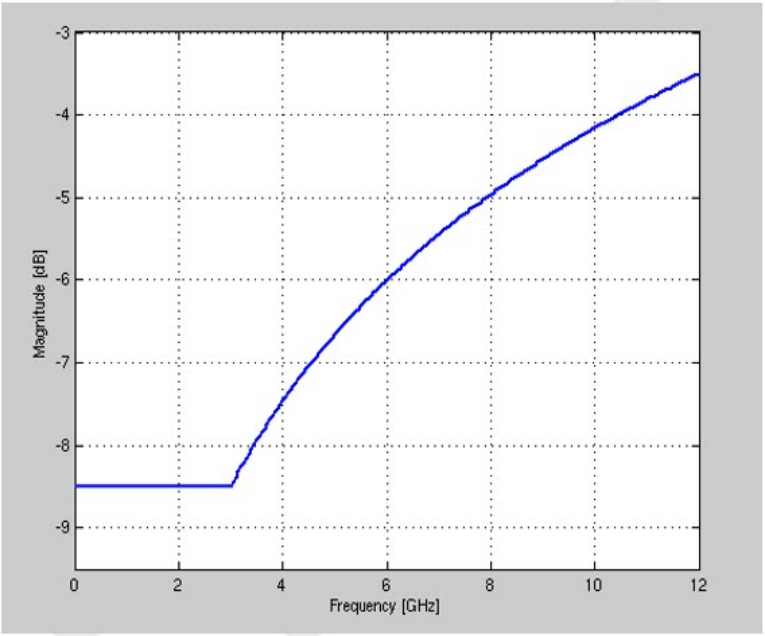
NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of this test is to confirm that the Differential Return Loss of a USB4 device is less than the maximum limit.

Test Pass Requirement

$$\mathrm{SDD11(f)} = \begin{cases} -8.5 & 0.05 < f_{GHz} \leq 3 \\ -3.5 + 8.3 \cdot \log 10\left(\frac{f_{GHz}}{12}\right) & 3 < f_{GHz} \leq 12 \end{cases}$$



Test Setup

1 For the physical connections between the DUT & the Oscilloscope, see the connection diagrams in Figure 73 and Figure 74.

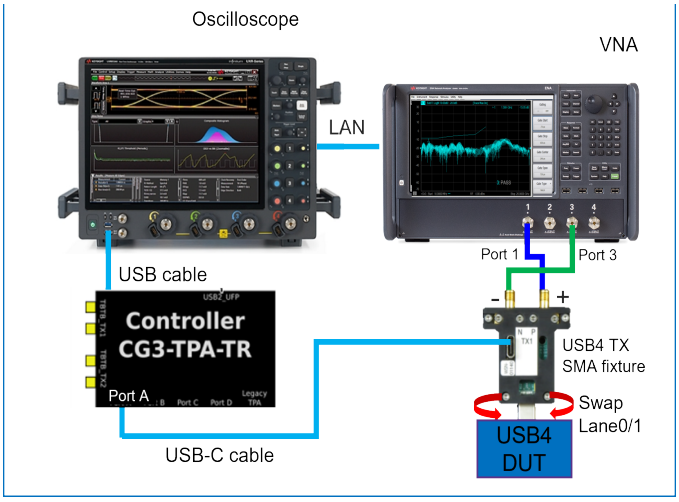


Figure 73 Tx Return loss test setup with Tx SMA test fixture

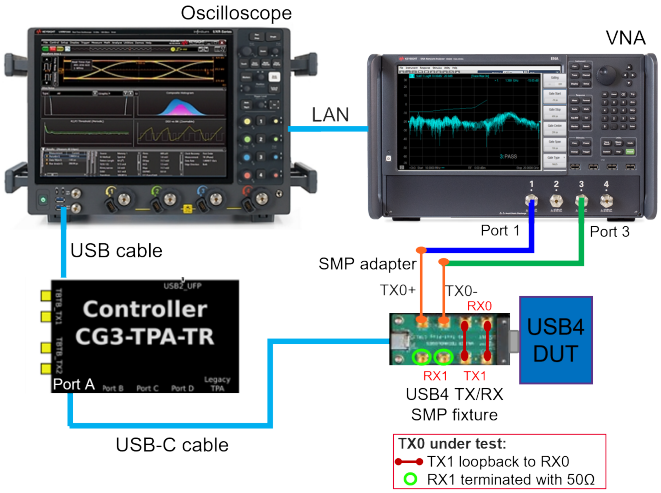
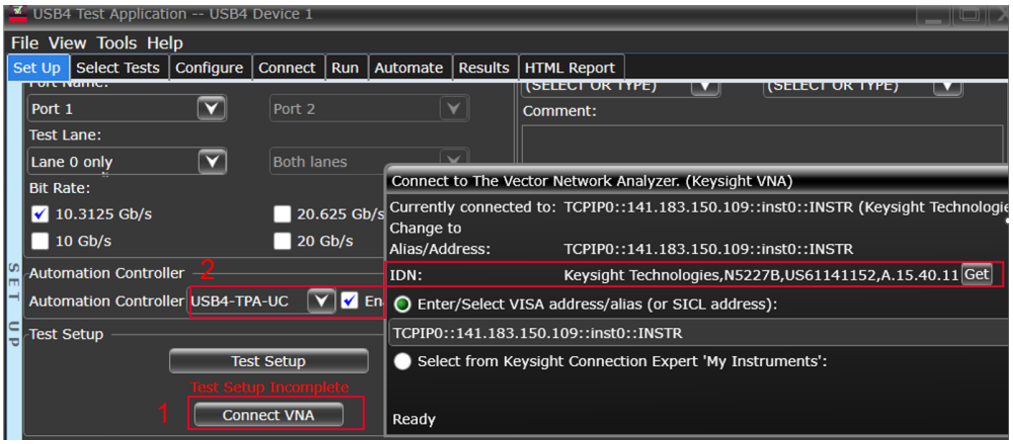


Figure 74 Return loss test setup with Tx/Rx SMP test fixture

2 In the **Set Up** tab, please connect VNA in the Tx app.

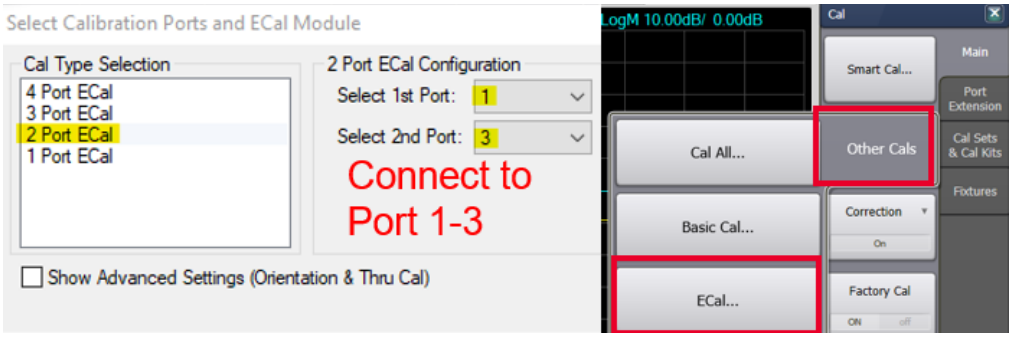


3 Prior calibration, setup Network Analyzer with following sweep settings:

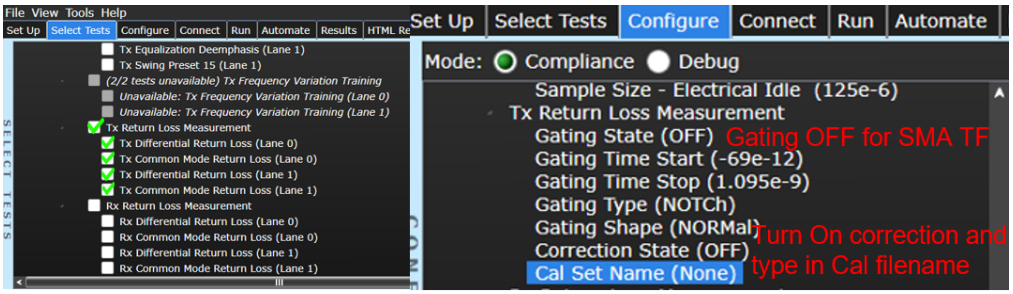
- Frequency range of 10 MHz to 12 GHz
- IF BW of 1 kHz
- At least 1600 points
- Impedance 85 ohm differential
- Define the Topology to Bal using VNA Port 1 and Port 3

NOTE Ensure that the VNA firmware revision is A.17.25.05 or higher to be compatible with the return loss test automation.

4 Run calibration on the network analyzer and test cables using a 2-port electronic kit (ECal). Save the Cal file.



5 In the **Select** test tab, select the Tx Return Loss Measurement and set the parameters in the **Configure** tab as shown in the figure below.



NOTE Please note that no gating setup is required for SMA fixture.

6 The test application sets USB4ETT **Tool Usage Mode**, commands VNA to measure Tx Return Loss in S2P, and compiles result using SigTest.

7 In the test setup, please flip the Tx fixture to swap the test lanes 0 and 1.

8 In case of SMP test fixture, Tx/Rx lane under test can be switched as shown in Figure 75.

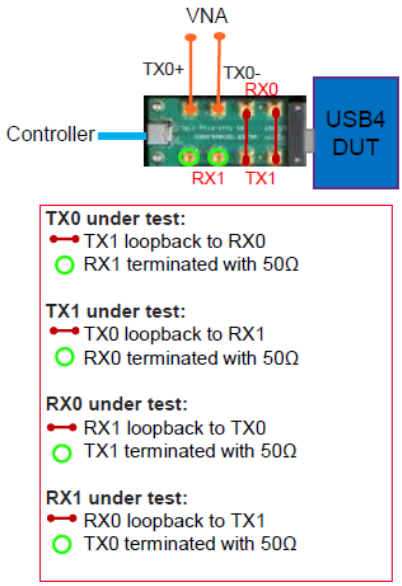


Figure 75 SMP test fixture - Tx/Rx lane switching

Test Procedure

1 Choose a supported USB4 speed to start with.
2 The test application sets USB4ETT tool to configure the DUT transmitter to output PRBS31 on all lanes with SSC turned on.
3 Connect Lane under test TX_P, TX_N to the Network Analyzer.
4 Measure the Differential R. Loss with the Network Analyzer and compile the result using SigTest.
5 If Differential Return loss violates the above requirement, then the result is Fail.
6 Repeat the test for all remaining USB4 lanes.
7 Repeat the test for all supported USB4 Gen2 and Gen3 speeds.

Expected / Observable Results

If Differential Return Loss violated the specified requirement, then Fail.

Test References

See

- *USB4 Specification Version 2.00, Table 3-2*

Tx Common Mode Return Loss Test

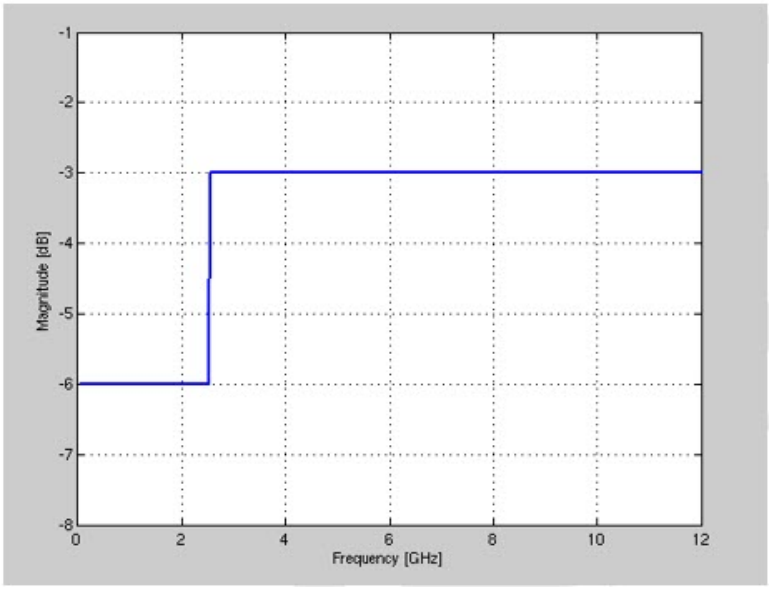
NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of this test is to confirm that the Common Mode Return Loss of a USB4 device is less than the maximum limit.

Test Pass Requirement

$$SCC11(f) = \begin{cases} -6 & 0.05 < f_{GHz} \leq 2.5 \\ -3 & 2.5 < f_{GHz} \leq 12 \end{cases}$$



Test Setup

1 For the physical connections between the DUT & the Oscilloscope, see the connection diagrams in Figure 76 and Figure 77.

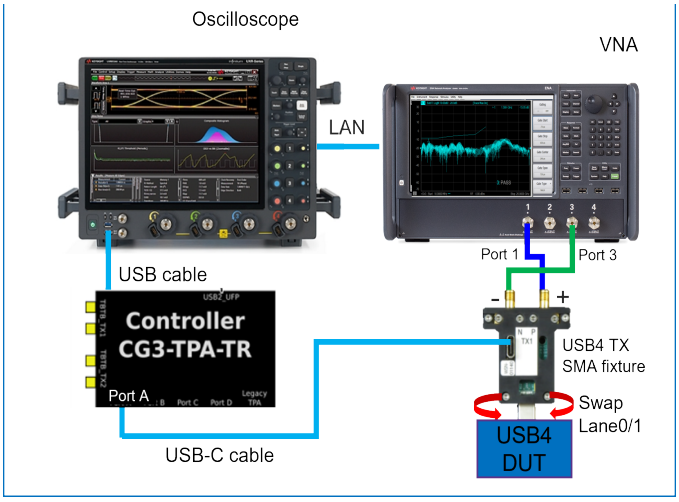


Figure 76 Tx Return loss test setup with Tx SMA test fixture

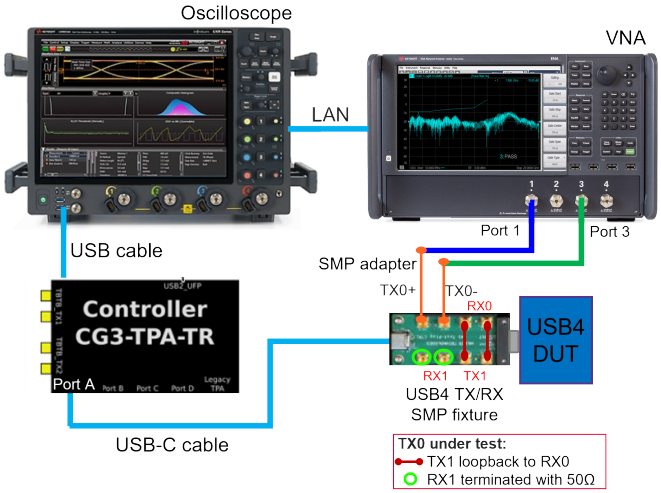
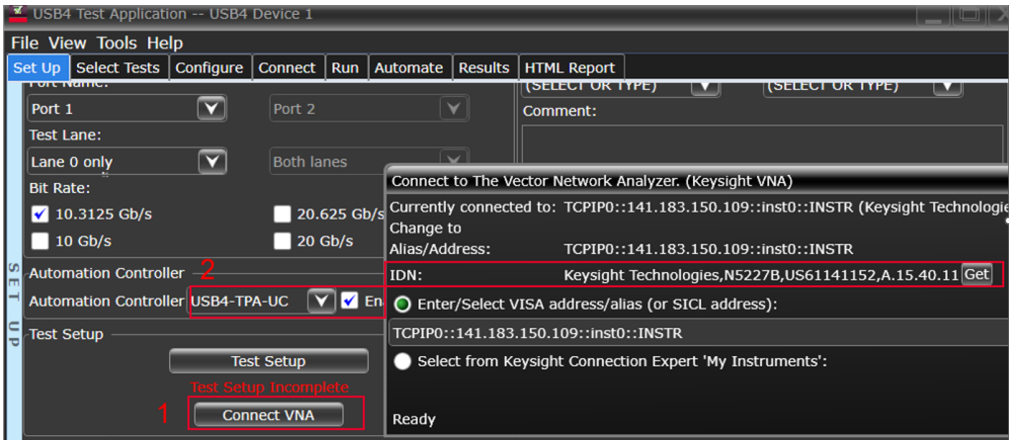


Figure 77 Return loss test setup with Tx/Rx SMP test fixture

2 In the **Set Up** tab, please connect VNA in the Tx app.

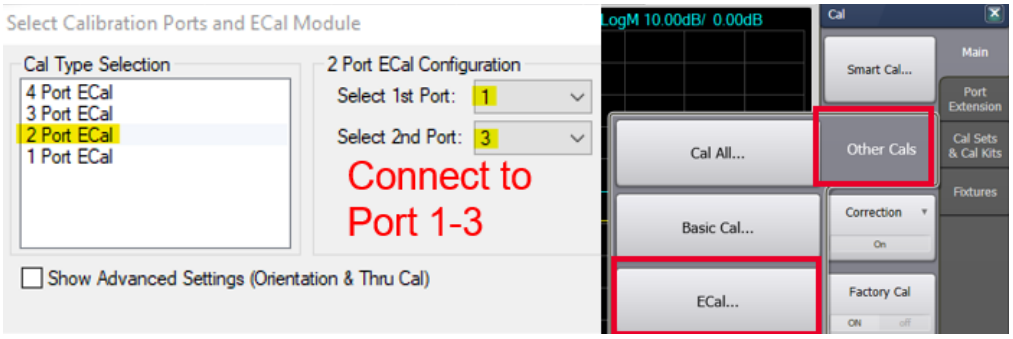


3 Prior calibration, setup Network Analyzer with following sweep settings:

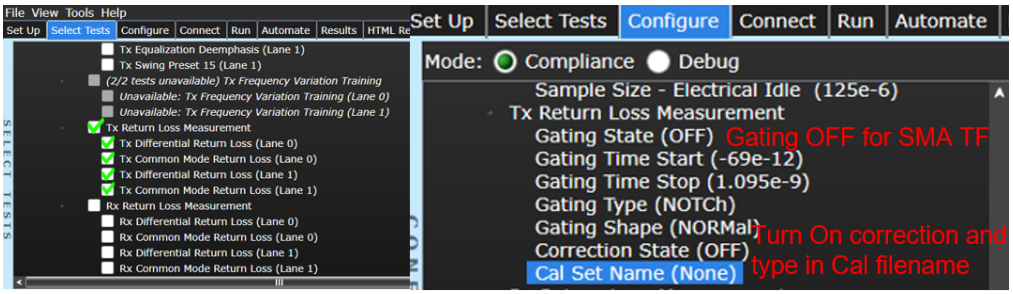
- Frequency range of 10 MHz to 12 GHz
- IF BW of 1 kHz
- At least 1600 points
- Impedance 85 ohm differential
- Define the Topology to Bal using VNA Port 1 and Port 3

NOTE Ensure that the VNA firmware revision is A.17.25.05 or higher to be compatible with the return loss test automation.

4 Run calibration on the network analyzer and test cables using a 2-port electronic kit (ECal). Save the Cal file.



5 In the **Select** test tab, select the Tx Return Loss test and set the parameters in the **Configure** tab as shown in the figure below.



NOTE Please note that no gating setup is required for SMA fixture.

6 The test application sets USB4ETT **Tool Usage Mode,** commands VNA to measure Tx Return Loss in S2P, and compiles result using SigTest.

7 In the test setup, please flip the Tx fixture to swap the test lanes 0 and 1.

8 In case of SMP test fixture, Tx/Rx lane under test can be switched as shown in Figure 78.

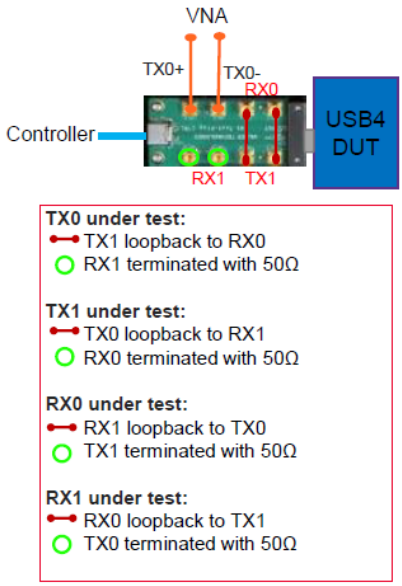


Figure 78 SMP test fixture - Tx/Rx lane switching

Test Procedure

1 Choose a supported USB4 speed to start with.
2 The test application sets USB4ETT tool to configure the DUT transmitter to output PRBS31 on all lanes with SSC turned on.
3 Connect Lane under test TX_P, TX_N to the Network Analyzer.
4 Measure the Common Mode Return Loss with the Network Analyzer and compile the result using SigTest.
5 If Common Mode Return loss violates the above requirement, then the result is Fail.
6 Repeat the test for all remaining USB4 lanes.
7 Repeat the test for all supported USB4 Gen2 and Gen3 speeds.

Expected / Observable Results

If Common Mode Return Loss violated the specified requirement, then Fail.

Test References

See

- *USB4 Specification Version 2.00, Table 3-2*

Rx Differential Return Loss Test

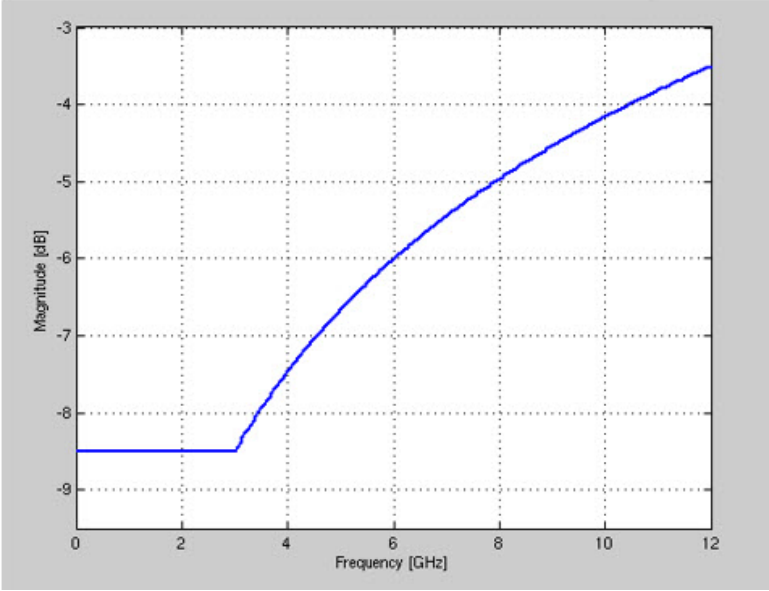
NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of this test is to confirm that the Differential Return Loss of a USB4 device is less than the maximum limit.

Test Pass Requirement

$$\mathrm{SDD22(f)} = \begin{cases} -8.5 & 0.05 < f_{GHz} \leq 3 \\ -3.5 + 8.3 \cdot \log 10\left(\frac{f_{GHz}}{12}\right) & 3 < f_{GHz} \leq 12 \end{cases}$$



Test Setup

1 For the physical connections between the DUT & the Oscilloscope, see the connection diagrams in Figure 79 and Figure 80.

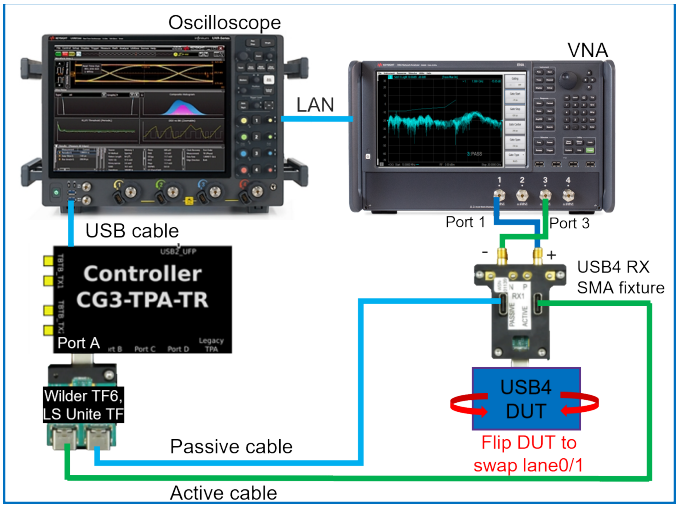


Figure 79 Tx Return loss test setup with Rx SMA test fixture

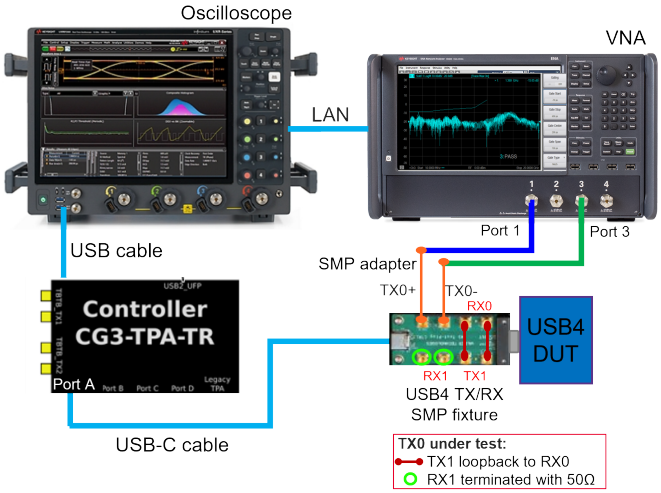
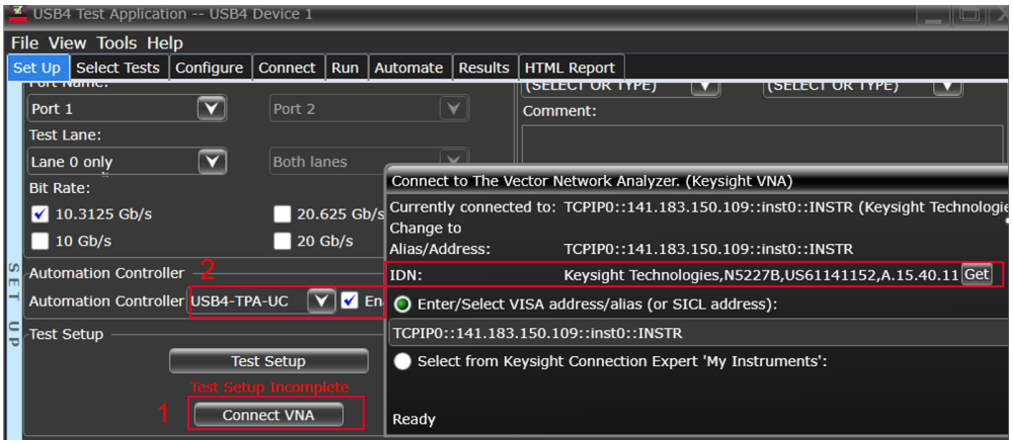


Figure 80 Return loss test setup with Tx/Rx SMP test fixture

2 In the **Set Up** tab, please connect VNA in the Tx app.

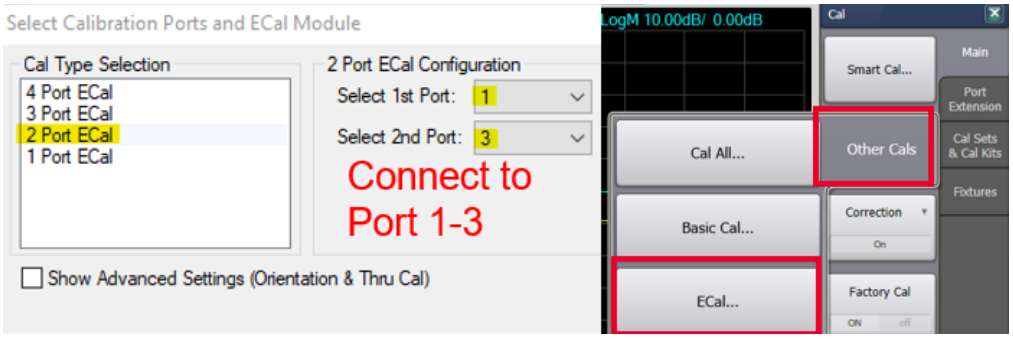


3 Prior calibration, setup Network Analyzer with following sweep settings:

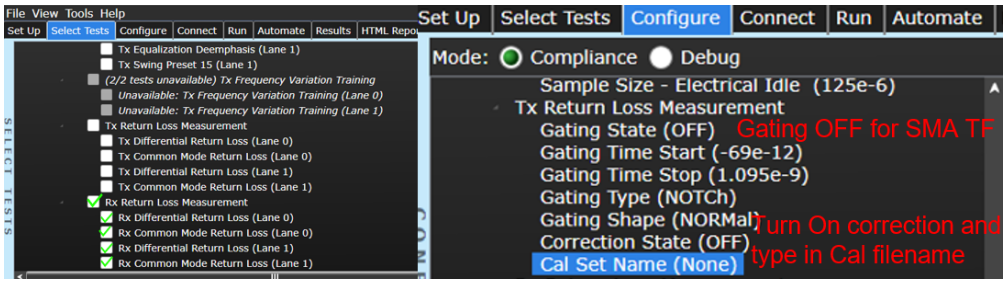
- Frequency range of 10 MHz to 12 GHz
- IF BW of 1 kHz
- At least 1600 points
- Impedance 85 ohm differential
- Define the Topology to Bal using VNA Port 1 and Port 3

NOTE Ensure that the VNA firmware revision is A.17.25.05 or higher to be compatible with the return loss test automation.

4 Run calibration on the network analyzer and test cables using a 2-port electronic kit (ECal). Save the Cal file.



5 In the **Select** test tab, select the Tx Return Loss test and set the parameters in the **Configure** tab as shown in the figure below.



NOTE Please note that no gating setup is required for SMA fixture.

6 The test application sets USB4ETT **Tool Usage Mode,** commands VNA to measure Tx Return Loss in S2P, and compiles result using SigTest.

7 In the test setup, please flip the Rx fixture to swap the test lanes 0 and 1.

8 In case of SMP test fixture, Tx/Rx lane under test can be switched as shown in Figure 81.

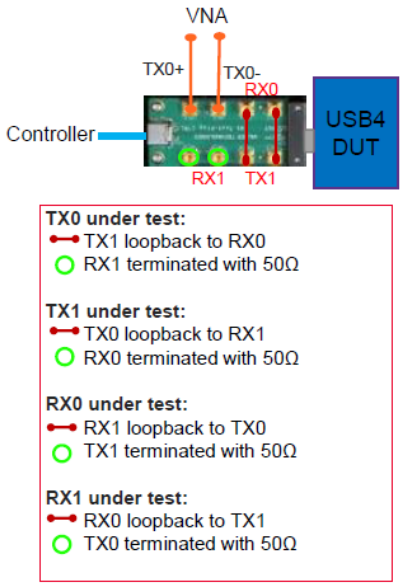


Figure 81 SMP test fixture - Tx/Rx lane switching

Test Procedure

1 Choose a supported USB4 speed to start with.
2 The test application sets USB4ETT tool to configure the DUT transmitter to output PRBS31 on all lanes with SSC turned on.
3 Connect a USB Type-C Passive cable from the Passive receptacle connector over the test fixture to the Low speed united coupon Passive receptacle connector that is connected to the USB4 Micro-controller PA.
4 Connect a USB Type-C Active cable from the Active receptacle connector over the test fixture to the Low speed united coupon Active receptacle connector that is connected to the USB4 Micro-controller PA.
5 Connect Lane under test RX_P, RX_N to the Network Analyzer.
6 Measure the Differential R. Loss with the Network Analyzer and compile the result using SigTest.
7 If Differential Return loss violates the above requirement, then the result is Fail.
8 Repeat the test for all remaining USB4 lanes.
9 Repeat the test for all supported USB4 Gen2 and Gen3 speeds.

Expected / Observable Results

If Differential Return Loss violated the specified requirement, then Fail.

Test References

See

- *USB4 Specification Version 2.00, Table 3-9*

Rx Common Mode Return Loss Test

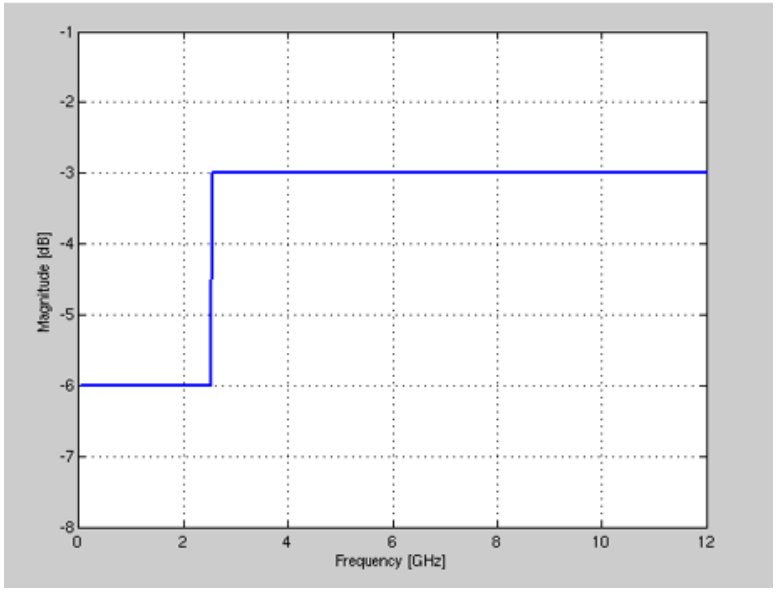
NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of this test is to confirm that the Common Mode Return Loss of a USB4 device is less than the maximum limit.

Test Pass Requirement

$$SCC22(f) = \begin{cases} -6 & 0.05 < f_{GHz} \leq 2.5 \\ -3 & 2.5 < f_{GHz} \leq 12 \end{cases}$$



Test Setup

1 For the physical connections between the DUT & the Oscilloscope, see the connection diagrams in Figure 82 and Figure 83.

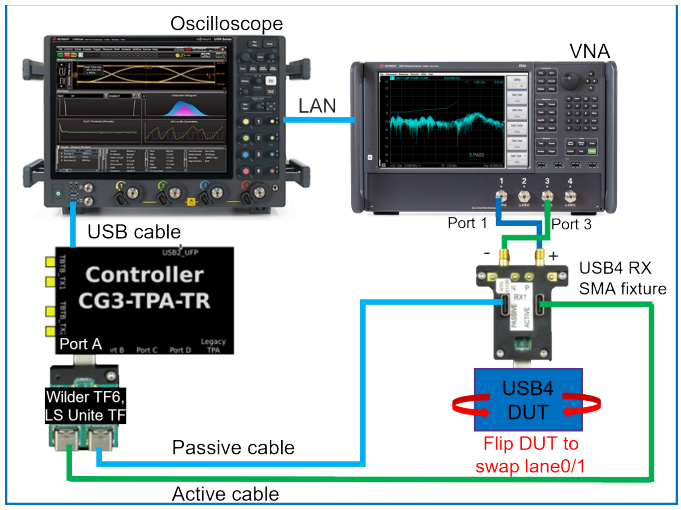


Figure 82 Tx Return loss test setup with Rx SMA test fixture

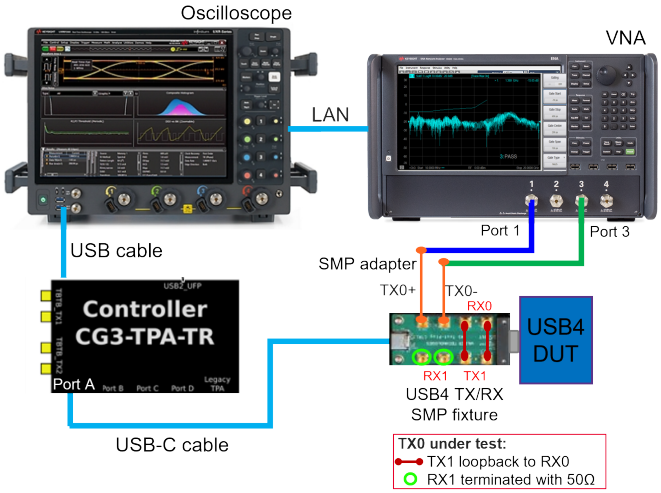
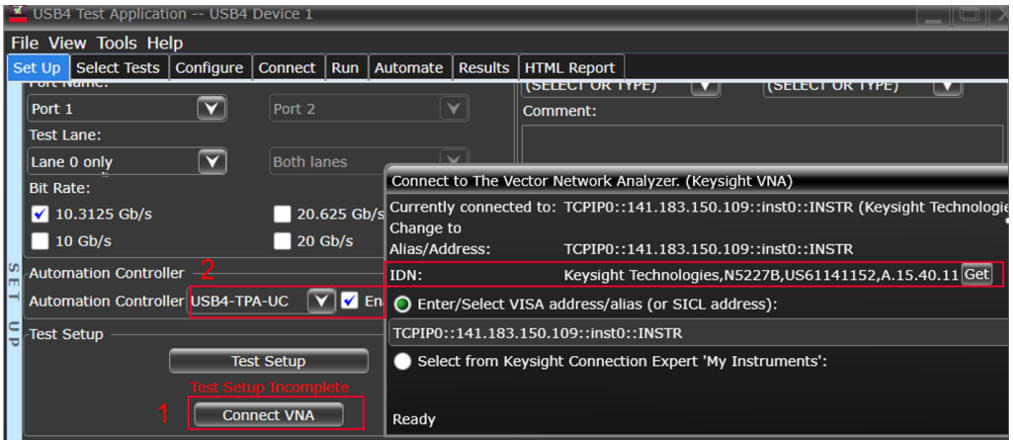


Figure 83 Return loss test setup with Tx/Rx SMP test fixture

2 In the **Set Up** tab, please connect VNA in the Tx app.

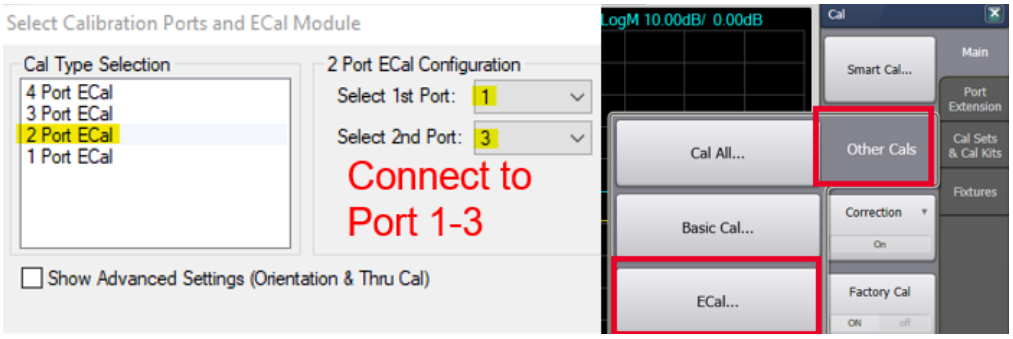


3 Prior calibration, setup Network Analyzer with following sweep settings:

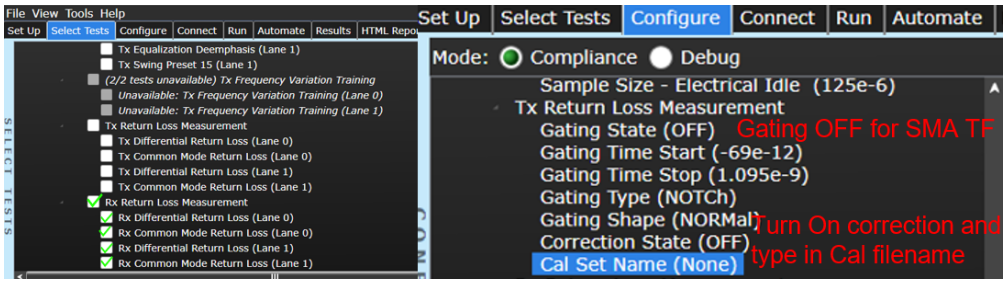
- Frequency range of 10 MHz to 12 GHz
- IF BW of 1 kHz
- At least 1600 points
- Impedance 85 ohm differential
- Define the Topology to Bal using VNA Port 1 and Port 3

NOTE Ensure that the VNA firmware revision is A.17.25.05 or higher to be compatible with the return loss test automation.

4 Run calibration on the network analyzer and test cables using a 2-port electronic kit (ECal). Save the Cal file.



5 In the **Select** test tab, select the Tx Return Loss test and set the parameters in the **Configure** tab as shown in the figure below.



NOTE Please note that no gating setup is required for SMA fixture.

6 The test application sets USB4ETT **Tool Usage Mode,** commands VNA to measure Tx Return Loss in S2P, and compiles result using SigTest.

7 In the test setup, please flip the Rx fixture to swap the test lanes 0 and 1.

8 In case of SMP test fixture, Tx/Rx lane under test can be switched as shown in Figure 84.

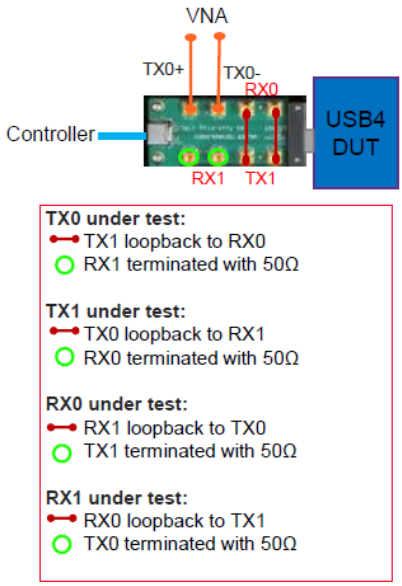


Figure 84 SMP test fixture - Tx/Rx lane switching

Test Procedure

1 Choose a supported USB4 speed to start with.
2 The test application sets USB4ETT tool to configure the DUT transmitter to output PRBS31 on all lanes with SSC turned on.
3 Connect a USB Type-C Passive cable from the Passive receptacle connector over the test fixture to the Low speed united coupon Passive receptacle connector that is connected to the USB4 Micro-controller.
4 Connect a USB Type-C Active cable from the Active receptacle connector over the test fixture to the Low speed united coupon Active receptacle connector that is connected to the USB4 Micro-controller.
5 Connect Lane under test RX_P, RX_N to the Network Analyzer.
6 Measure the Common Mode Return Loss with the Network Analyzer and compile the result using SigTest.
7 If Common Mode Return loss violates the above requirement, then the result is Fail.
8 Repeat the test for all remaining USB4 lanes.
9 Repeat the test for all supported USB4 Gen2 and Gen3 speeds.

Expected / Observable Results

If Common Mode Return Loss violated the specified requirement, then Fail.

Test References

See

- *USB4 Specification Version 2.00, Table 3-9*

6 Transmitter Tests for 10 GB/s Systems

Tx Preset Calibration / 178
SBTX High Voltage / 182
SBTX Low Voltage / 184
SBTX Rise/Fall Time / 186
SBTX UI Duration / 189
SBRX High Voltage Detection / 192
SBRX Low Voltage Detection / 194
Tx Rise/Fall Time / 195
Tx Uncorrelated Jitter / 197
Tx Uncorrelated Deterministic Jitter / 199
Tx Data Dependent Jitter / 201
Tx Duty Cycle Distortion / 203
Tx Low Frequency Uncorrelated Deterministic Jitter / 205
Tx Total Jitter / 207
Tx Uncorrelated Jitter TP3 / 209
Tx Uncorrelated Deterministic Jitter TP3 / 211
Tx Total Jitter TP3 / 213
Tx Eye Diagram TP3 / 216
Tx Minimum Unit Interval, Min/Max / 219
Tx SSC Down Spread Rate / 221
Tx SSC Down Spread Range / 223
Tx SSC Slew Rate / 225
Tx SSC Phase Deviation / 227
Tx Eye Diagram / 229
Tx AC Common Mode Voltage / 231
Tx Equalization Tests / 233
Tx Electrical Idle Voltage Test / 238
Tx Differential Return Loss Test / 240
Tx Common Mode Return Loss Test / 245
Rx Differential Return Loss Test / 250
Rx Common Mode Return Loss Test / 255

This section provides the Methods of Implementation (MOIs) to run electrical tests on a USB DUT operating at a bit rate of 10 GB/s using a Keysight Infiniium Oscilloscope and other accessories, along with the USB4 Test Application.

NOTE All USB4 devices that support a bit rate of 10 Gb/s are classified as Gen2 devices.

Tx Preset Calibration

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Preset Calibration Test is to find the optimized preset for the platform.

NOTE Prior to running the compliance tests, the Host / Device must go through Preset Calibration.

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 86 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Preset Calibration* are checked.

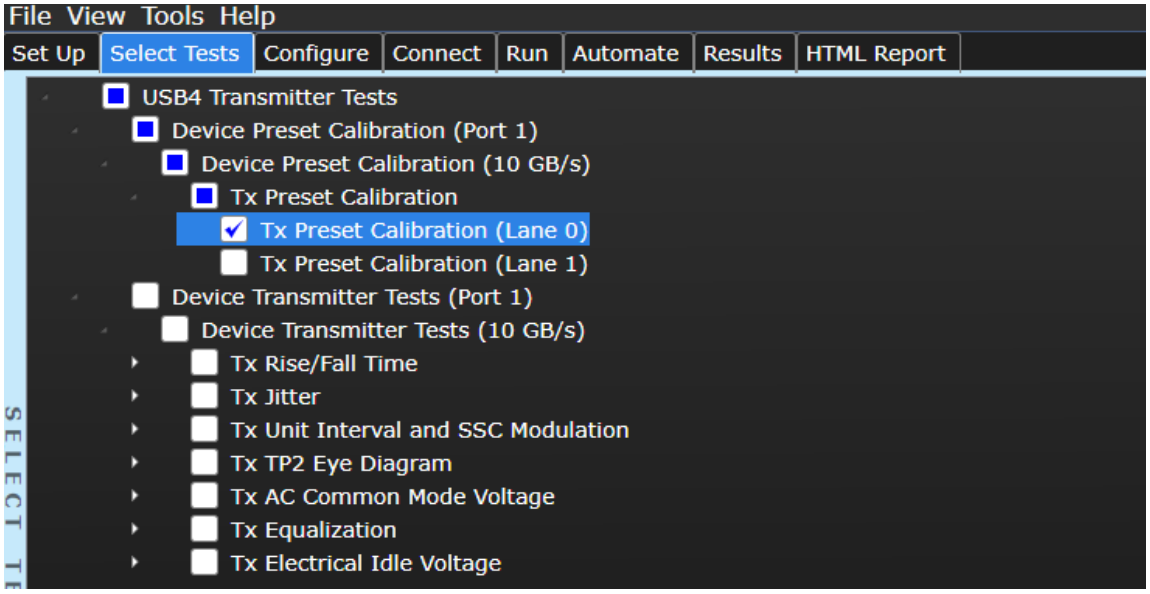


Figure 85 Selecting the Tx Preset Calibration tests

NOTE

By default, the test group for **Preset Calibration** for each selected bit-rate is hidden in the **Select Tests** tab when **Predefined Optimum Preset Number** is selected for the respective bit-rates. To view and select the **Preset Calibration** tests in the **Select Tests** tab, select the **Run Preset Calibration** option in the **Test Setup** window of the **Set Up** tab.

NOTE

In the **Measurement Server** mode or **Multi** instance mode, it is recommended to run the **Tx Preset Calibration** tests first to get the optimized preset value. Then use this value to run the remaining transmitter tests.

Detailed Process:

In the **Measurement Server** mode or **Multi** instance mode, after running the **Preset Calibration** test, please see the HTML Report and note down the optimized preset value. Then, please navigate to **Set Up** tab > **Test Setup** button > **Test Setup** dialog box. Select the check box “Predefined Optimum Preset Number”, use the already noted optimized preset number, and manually **Select the Optimum Preset Number for Each Bit Rate**. Now, please run the rest of the transmitter tests.

USB4 Microcontroller and Test Adapter USB Test Set-up

The figure, below, shows a simplified set-up example of a USB4 Microcontroller and a US4B Test Adapter used to test a typical USB DUT.

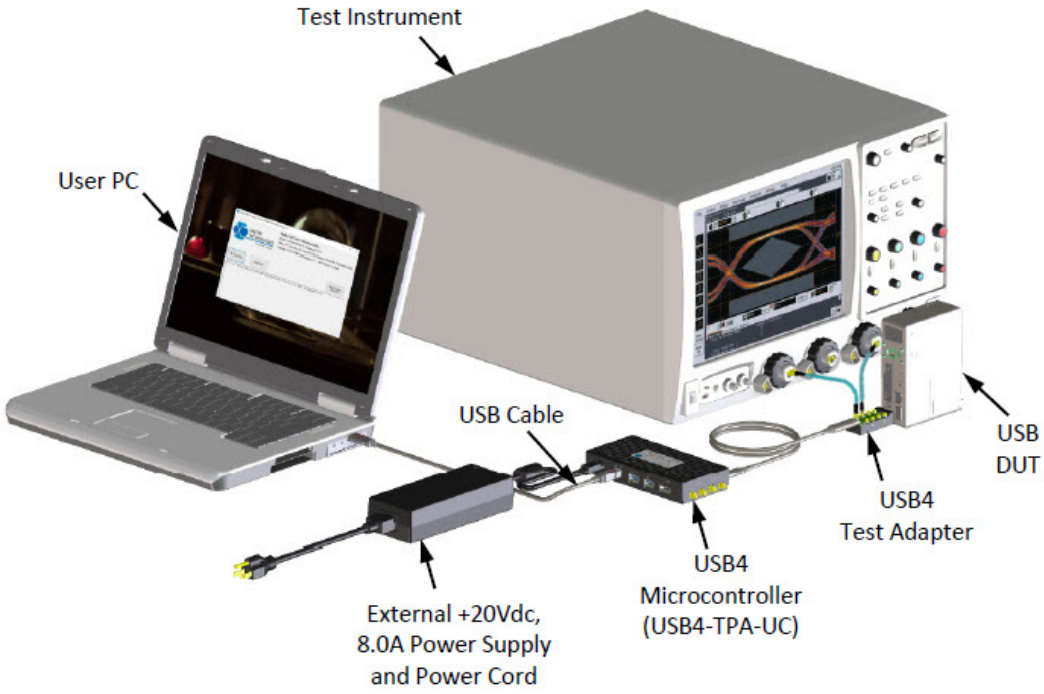


Figure 86 Transmitter TP2/TP3 Test Setup

Test Procedure

1 Connect the DUT to the Oscilloscope as shown in the Figure 86.
2 Choose a USB4 speed to start with.
3 Configure the DUT transmitter to output PRBS15, preset 0 on all lanes with SSC enabled.
4 The cables from the plug test fixture to the scope shall be de-embedded.
5 Perform measurements with:
   a Reference CDR modeled by a 2^{nd} order PLL response which drives High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used.
   b Oscilloscope with a minimum bandwidth of 16 GHz.
6 Capture the waveform and process it with the digital oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Evaluate 40 Mpts per channel when using 80 GSa/s. For higher sample rate use memory depth in the same ration to 40 Mpts.
   c Pattern length - Periodic
   d Jitter separation method shall be suitable for cross talk on signal
   e Adjust vertical scale to fit signal into scope screen.
   f Referenced to 1E-13 statistics.
7 Capture DDJ results for lane 0.
8 Repeat the test for all remaining USB4 transmit presets (till preset 15 as shown in Table 5).
9 Repeat the test for the remaining USB4 lanes.
10 For each lane, choose the preset that provides minimum DDJ.
11 Repeat the above procedure for all supported USB4 speeds.

Expected / Observable Results

For each lane, the preset that provides the minimum DDJ is the optimized preset for the platform.

Test References

See

- USB4 Specification Version 2.00 (Table 3-5)

SBTX High Voltage

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of this test is to confirm that the SBTX High Voltage Measurement of a USB4 device is within the specification limits.

Test Pass Requirement

2.40 V ≤ SBTX High Voltage Measurement ≤ 3.52 V

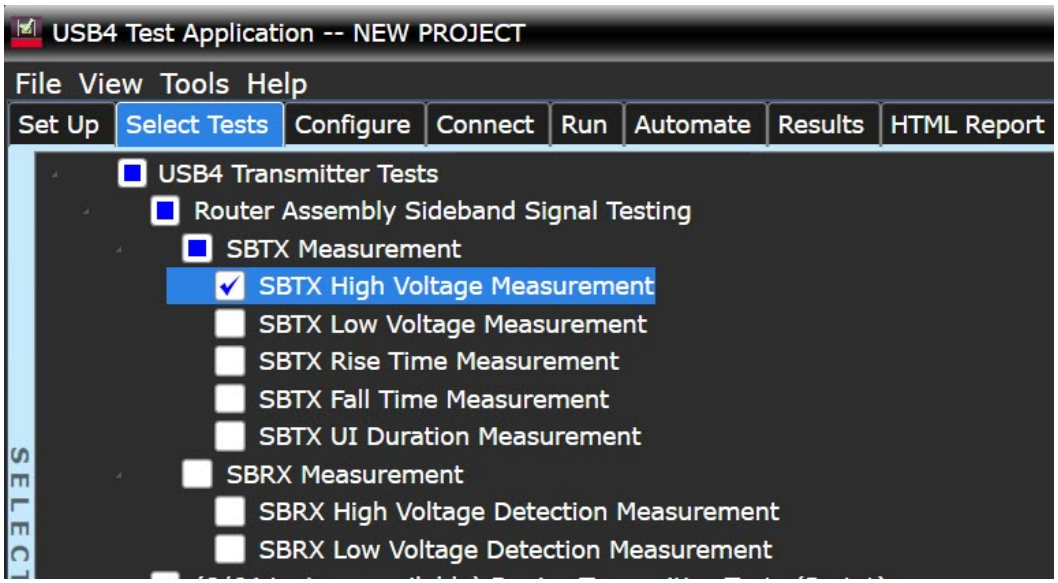
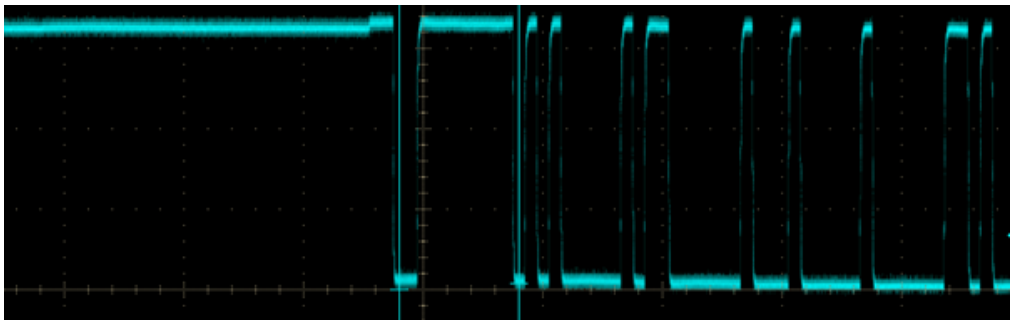


Figure 87 Selecting the SBTX High Voltage Measurement test

Test Procedure

1. Connect a voltage meter/DMMfluke to SBU1 header in the USB4 Test Fixture.
2. Power up the DUT.
3. Measure the voltage.
4. If $SBTX_{VOH}$ < 2.4 V or > 3.52 V then Fail.
5. Connect a scope with high impedance probe to the SBU1 header in the USB4 Test Fixture.
6. In the scope use a trigger based on pulse width, negative polarity, trigger when the pulse width <10 µs and threshold of 600 mV.
7. Horizontal scale = 10 µs per square, vertical scale = 1 V per square.
8. Power up the DUT.

9 Over the Infiniium Oscilloscope the trigger shall capture the transaction pattern.



10 Measure the high/low value of the "1" amplitude for a bit inside the transaction. Over/undershoot shall be ignored.

11 If $SBTX_{VOH}$ < 2.4 V or > 3.52 V then Fail.

Expected / Observable Results

If $SBTX_{VOH}$ < 2.4 V or > 3.52 V then Fail.

Test References

See

- *USB4 Specification Version 2.00 (Table 3-32)*

SBTX Low Voltage

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of this test is to confirm that the SBTX Low Voltage Measurement of a USB4 device is within the specification limits.

Test Pass Requirement

2.40 V ≤ SBTX Low Voltage Measurement ≤ 3.52 V

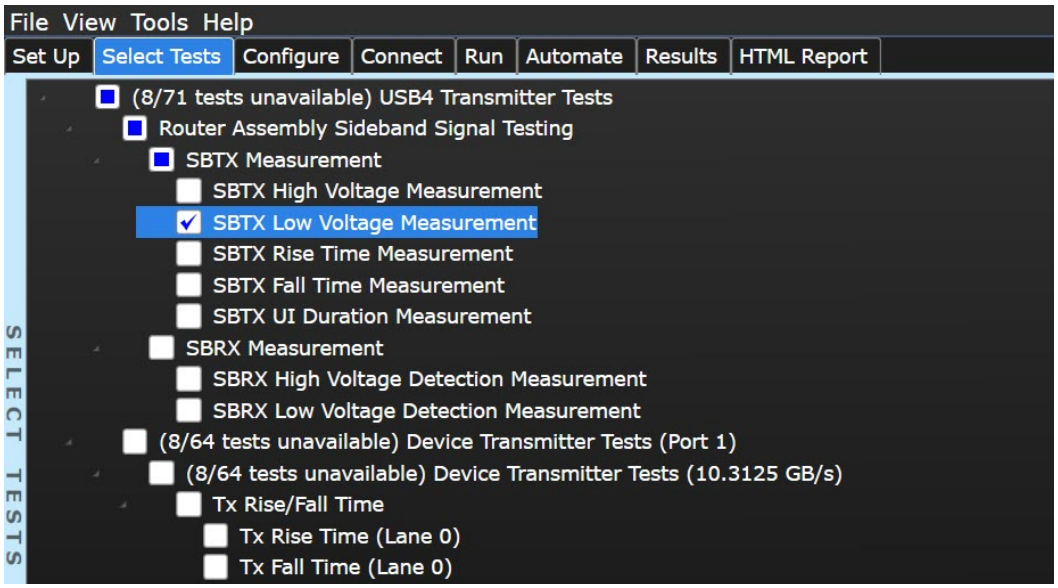


Figure 88 Selecting the SBTX Low Voltage Measurement test

Test Procedure

1. Connect a voltage meter/DMMfluke to SBU1 header in the USB4 Test Fixture.
2. DUT shall be in power down state.
3. Measure the voltage.
4. If $SBTX_{VOL}$ < -0.05 V or > 0.4 V then Fail.
5. Connect a scope with high impedance probe to the SBU1 header in the USB4 Test Fixture.
6. In the scope use a trigger based on pulse width, negative polarity, trigger when the pulse width <10 µs and threshold of 600 mV.
7. Horizontal scale = 10 µs per square, vertical scale = 1 V per square.
8. Connect link partner to the DUT.
9. Over the Infiniium Oscilloscope the trigger shall capture the transaction pattern.

10 Measure the high/low value of the "0" amplitude for a bit inside the transaction. Over/undershoot shall be ignored.

11 If $SBTX_{VOL}$ < -0.05 V or > 0.4 V then Fail.

Expected / Observable Results

If $SBTX_{VOL}$ < -0.05 V or > 0.4 V then Fail.

Test References

See

- *USB4 Specification Version 2.00 (Table 3-32)*

SBTX Rise/Fall Time

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of this test is to confirm that the SBTX Rise/Fall Time Measurement of a USB4 device is within the specification limits.

Test Pass Requirement

$3.5\ ns \leq SBX_{TRTF} \leq 65\ ns$.

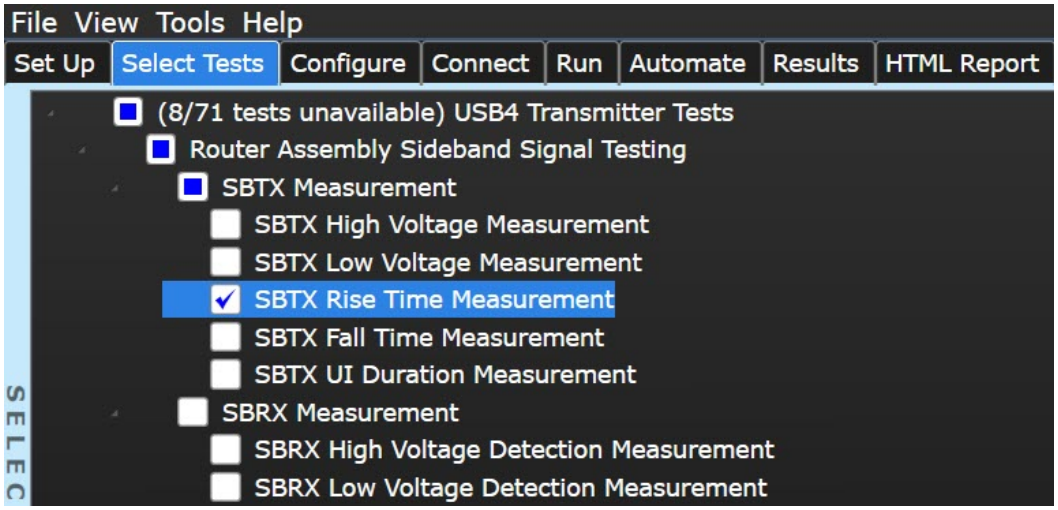


Figure 89 Selecting the SBTX Rise Time Measurement test

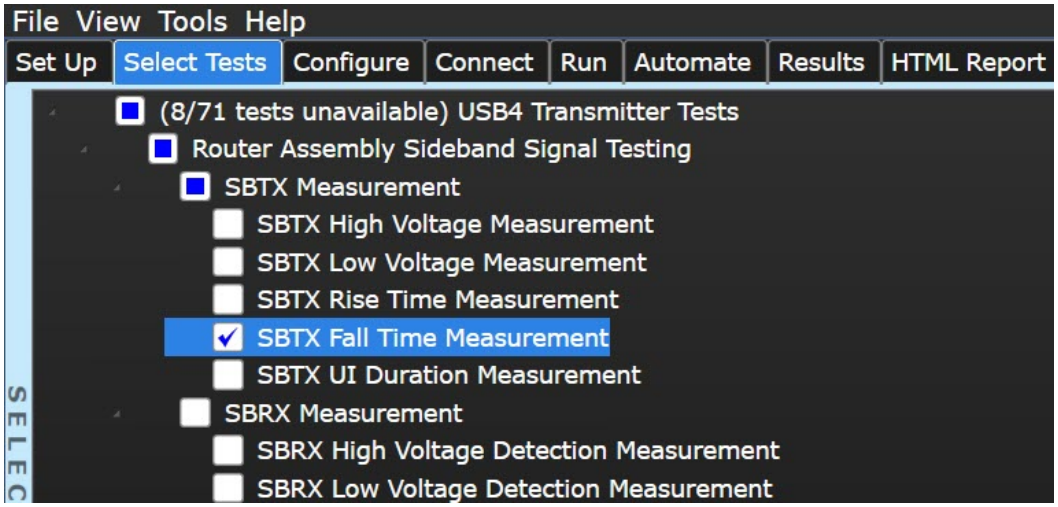
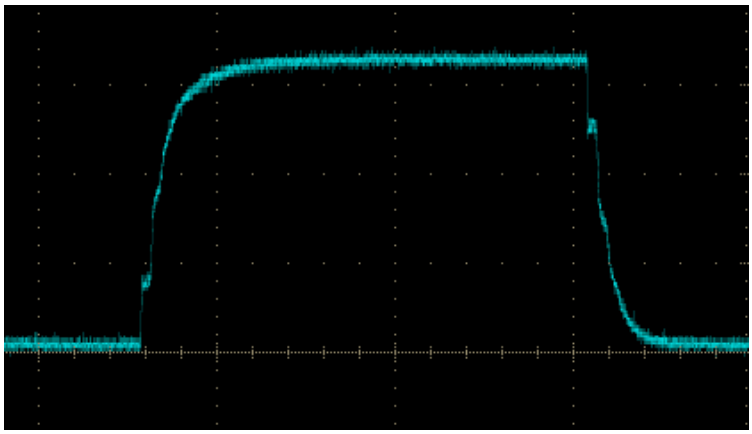


Figure 90 Selecting the SBTX Fall Time Measurement test

Test Procedure

1 Connect the DUT via USB4 Test Fixture with USB4 u-controller in order to establish link.
2 The measurement shall be in transaction only and not from power down to up (or the opposite).
3 Connect a scope with high impedance probe to the SBU1 header for SBTX test in the USB4 Test Fixture.
4 In the scope use a trigger based on pulse width, negative polarity, trigger when the pulse width <10 µs and threshold of 600 mV.
5 Horizontal scale = 10 µs per square, vertical scale = 1 V per square.
6 Power up the DUT.
7 Over the Infiniium Oscilloscope the trigger shall capture the transaction pattern.
8 Zoom in one bit from inside the transaction pattern. Not the 1st or the last bit.



9 Measure the rise and fall time (10%-90%) for SBTX.
10 If 65 ns < STX_{TRTF} < 3.5 ns then Fail.

Expected / Observable Results

If 65 ns < STX_{TRTF} < 3.5 ns then Fail.

Test References

See

- *USB4 Specification Version 2.00 (Table 3-32)*

SBTX UI Duration

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of this test is to confirm that the SBTX UI Duration Measurement of a USB4 device is within the specification limits.

Test Pass Requirement

970 ns ≤ SBX_{UI} ≤ 1030 ns.

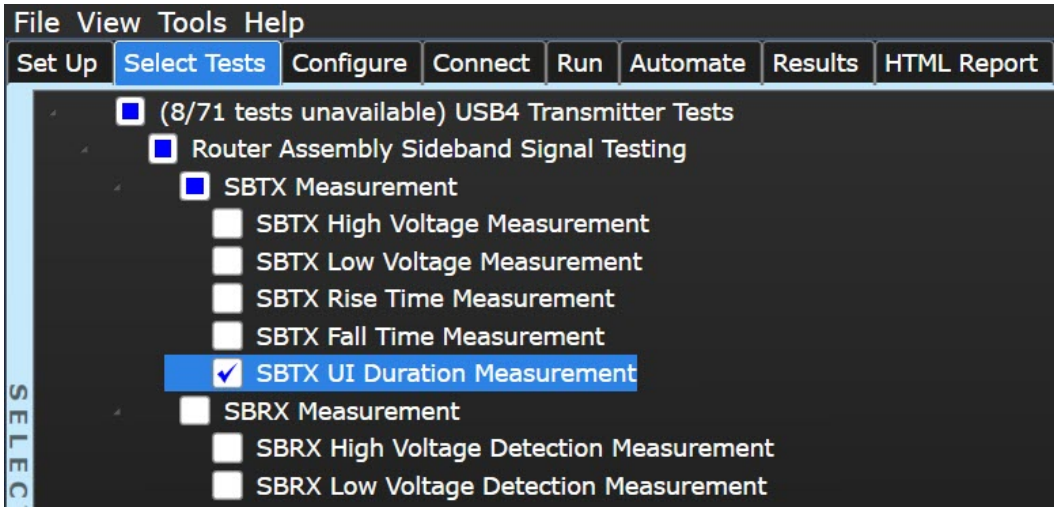
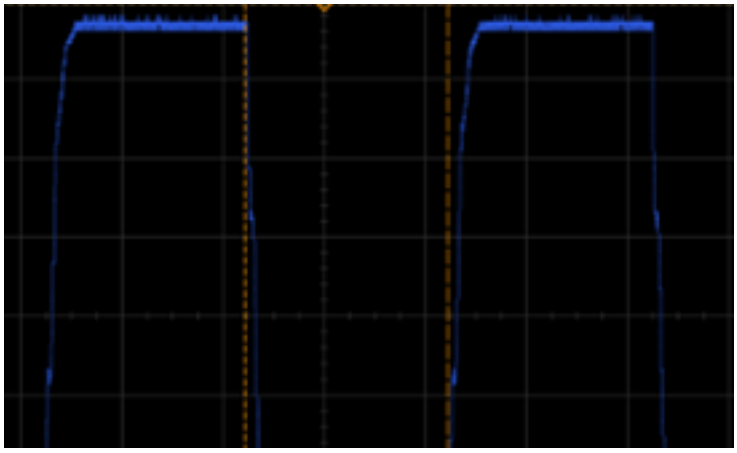


Figure 91 Selecting the SBTX UI Duration Measurement test

Test Procedure

1 Connect the DUT via USB4 Test Fixture with USB4 u-controller in order to establish link.
2 The measurement shall be in transaction only, over the transaction pattern.
3 Connect a scope with high impedance probe to the SBU1 header for SBTX test in the USB4 Test Fixture.
4 In the scope use a trigger based on pulse width, negative polarity, trigger when the pulse width <10 µs and threshold of 600 mV.
5 Horizontal scale = 10 µs per square, vertical scale = 1 V per square.
6 Power up the DUT.
7 Over the Infiniium Oscilloscope the trigger shall capture the transaction pattern.
8 Zoom in "10" bits from the transaction pattern.



9 Measure the duration from falling edge of the "1" to the rising edge of "0", named SBX_UI.
10 If 970 ns < $SBTX_{UI}$ < 1030 ns then Fail.

Expected / Observable Results

If 970 ns < $SBTX_{UI}$ < 1030 ns then Fail.

Test References

See

- *USB4 Specification Version 2.00 (Table 3-32)*

SBRX High Voltage Detection

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of this test is to confirm that the SBRX High Voltage Detection Measurement of a USB4 device is within the specification limits.

Test Pass Requirement

$2.0\ V \leq SBRX_{VIH} \leq 3.77\ V$

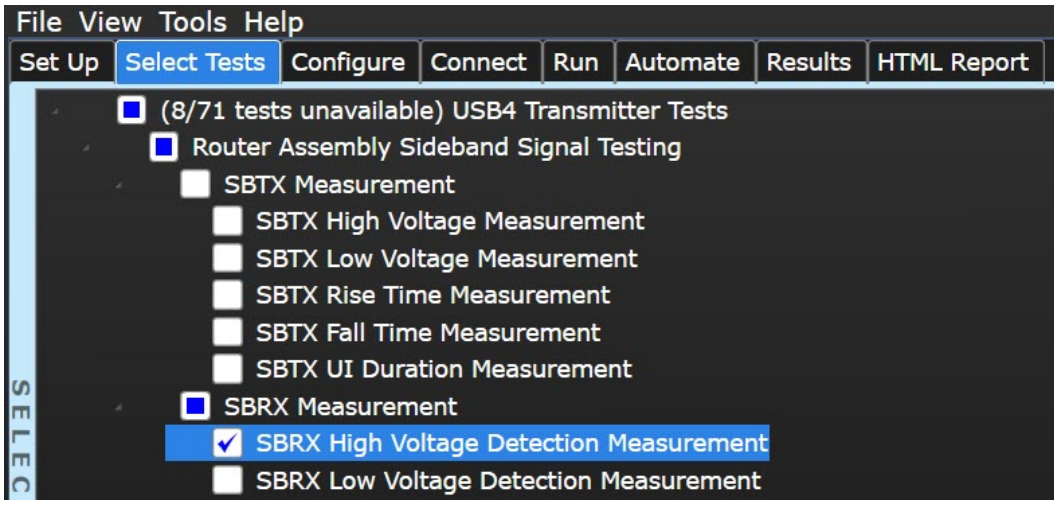
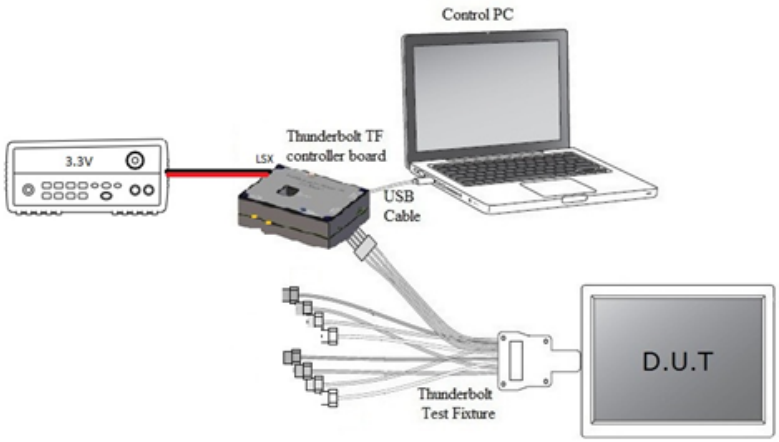


Figure 92 Selecting the SBRX High Voltage Measurement test

Test Procedure

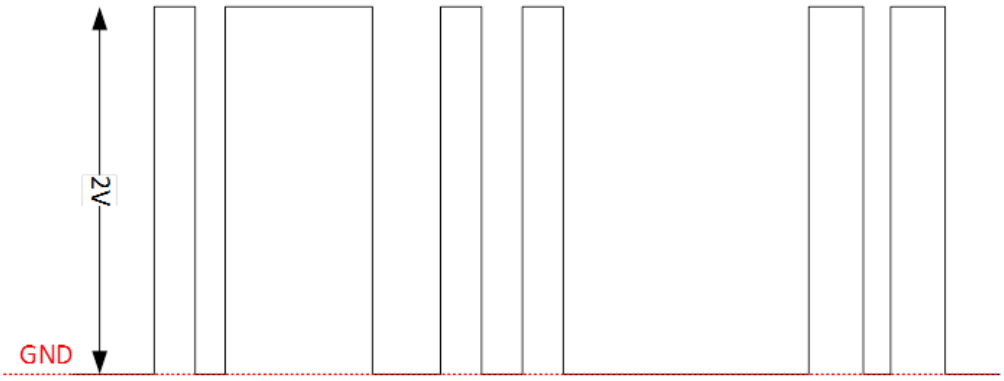
1 Connect the DUT via USB4 LSXX Test Fixture with USB4 u-controller and set '1' bit amplitude to 3.3 V and '0' bit amplitude to 0 V in order to establish link.



2 Set the 3.3 V power supply to 3.77 V.

3 Establish there is a link.

4 Reduce the external power supply to 2.0 V.



5 If link is lost, then Fail.

Expected / Observable Results

2.0 V ≤ $SBRX_{VIH}$ ≤ 3.77 V

Test References

See

- *USB4 Specification Version 2.00 (Table 3-32)*

SBRX Low Voltage Detection

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of this test is to confirm that the SBRX Low Voltage Detection Measurement of a USB4 device is within the specification limits.

Test Pass Requirement

$-0.3\ V \leq SBRX_{VIL} \leq 0.65\ V$

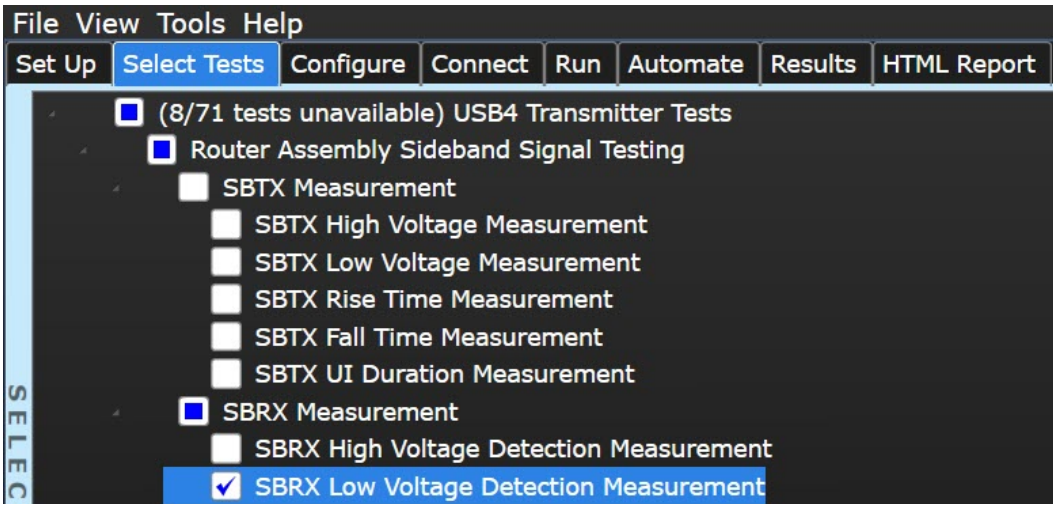


Figure 93 Selecting the SBRX Low Voltage Measurement test

Test Procedure

1. Connect the DUT via USB4 Test Fixture with USB4 u-controller with external 3.3 V power supply connected to the SBX input in order to establish link.
2. Set the 3.3 V power supply to 3.3 V.
3. Establish there is a link.
4. Reduce the external power supply to 0.65 V.
5. If link is established, then Fail.

Expected / Observable Results

$-0.3\ V \leq SBRX_{VIL} \leq 0.65\ V$

Test References

See

- *USB4 Specification Version 2.00 (Table 3-32)*

Tx Rise/Fall Time

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Rise/Fall Time Test is to confirm that the rise times and fall times on the USB differential signals are within the limits of the specification.

Test Pass Requirement

Rise Time and Fall Time $\geq$ 10.00 ps (Refer to Table 3 on page 74).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 86 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Rise/Fall Time* are checked.

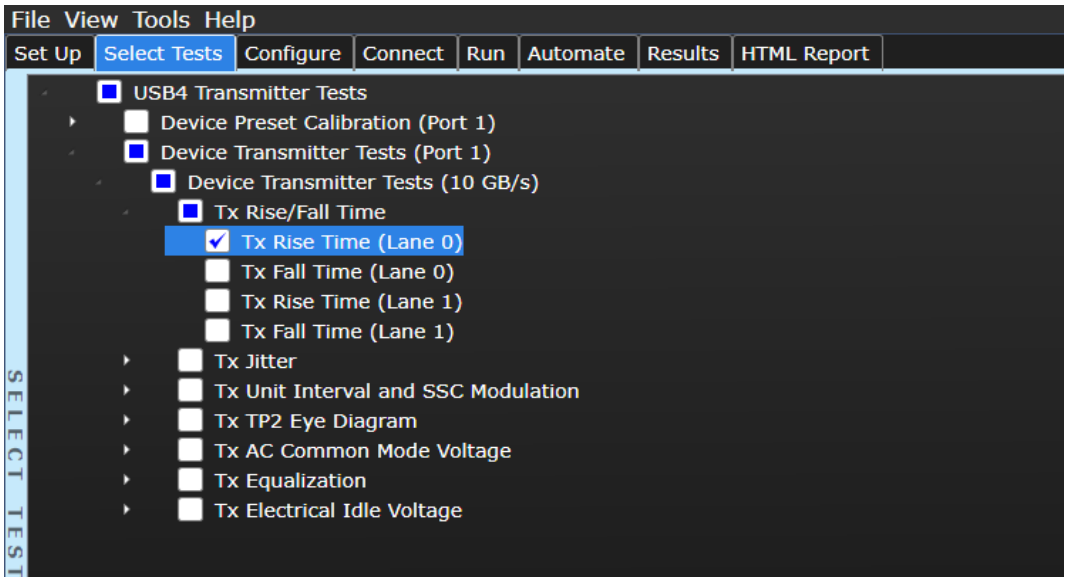


Figure 94 Selecting the Tx Rise/Fall Time tests

Test Procedure

1 Configure DUT transmitter to output alternating square pattern of 64 0's and 64 1's (SQ128) on all lanes with SSC turned on.
2 Evaluate at least 4Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ratio to 4Mpts. Use the maximum analog bandwidth of the Oscilloscope.

   No CDR, no average and no interpolation to be used.

   Adjust vertical scale such that the signal fits within the Oscilloscope's display.
3 Measure T_{RISE} as the mode of the sampled edge times from 20% to 80% of the differential swing voltage rising edge.
4 Measure T_{FALL} as the mode of the sampled edge times from 80% to 20% of the differential swing voltage falling edge.
5 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If T_{RISE} < 10.00 ps, the status of test is FAIL.

If T_{FALL} < 10.00 ps, the status of test is FAIL.

Test References

See

- *USB4 Specification Version 2.00 (Table 3-2)*

Tx Uncorrelated Jitter

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Uncorrelated Jitter Test is to confirm that the Uncorrelated Jitter [Deterministic Jitter (DJ) and Random Jitter (RJ) components] of the transmitter is within the limits of the specification.

Test Pass Requirement

Uncorrelated Jitter (UJ) $\leq$ 0.31 UI_{p-p} (Refer to Table 6 on page 83).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 86 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter, Data Dependent Jitter and Duty Cycle Distortion* are checked.

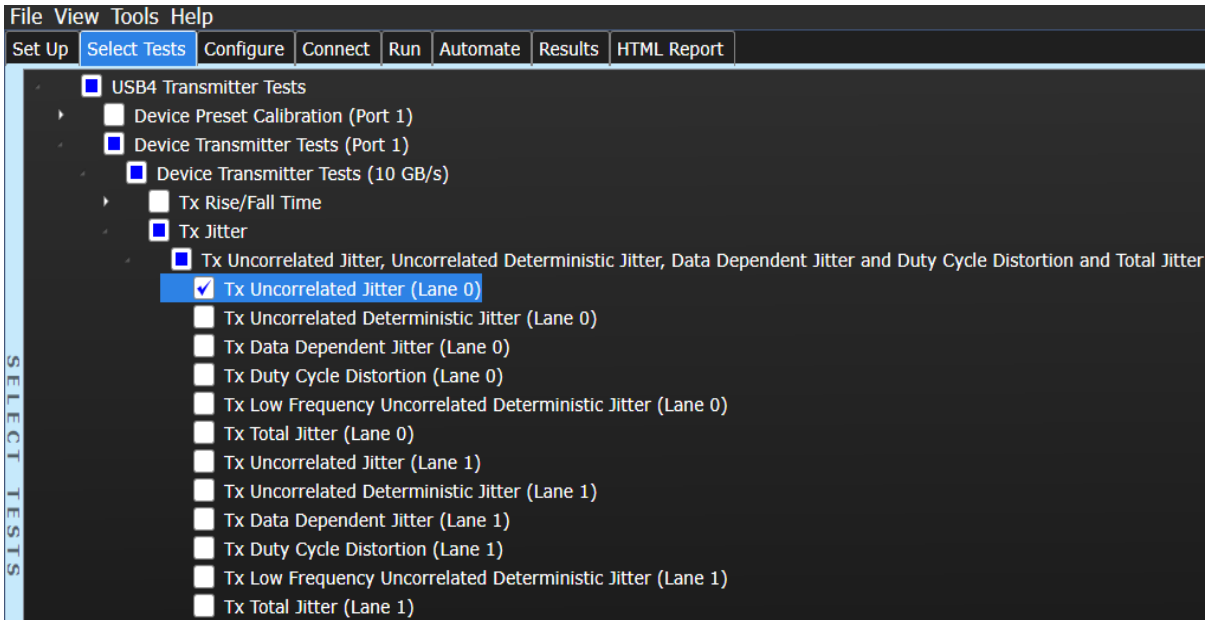


Figure 95 Selecting the Tx Sum of Uncorrelated Jitter tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2 Perform measurements with:
   a Reference CDR based on the 2^{nd} order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   b Oscilloscope with a minimum bandwidth of 16GHz
3 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Pattern length – Periodic
   c Jitter Separatio method must be suitable for cross-talk on the signal
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Evaluate 40 Mpts per channel when using 80 GSa/s. For higher sample rates, use memory depth in the same ratio to 40 Mpts
   f Referenced to 1E-13 statistics
4 Capture the Total Jitter (TJ) and Data Dependent Jitter (DDJ) results.
5 Calculate UJ using the equation:

$$UJ = TJ - DDJ$$

6 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If UJ > 0.31 UI_{p-p}, the status of test is FAIL.

Test References

See

- *USB4 Specification Version 2.00 (Table 3-5)*

Tx Uncorrelated Deterministic Jitter

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Uncorrelated Deterministic Jitter Test is to confirm that the Uncorrelated Deterministic Jitter of the transmitter is within the limits of the specification.

Test Pass Requirement

Uncorrelated Deterministic Jitter (UDJ) $\leq$ 0.17 UI_{p-p} (Refer to Table 6 on page 83).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 86 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter, Data Dependent Jitter and Duty Cycle Distortion* are checked.

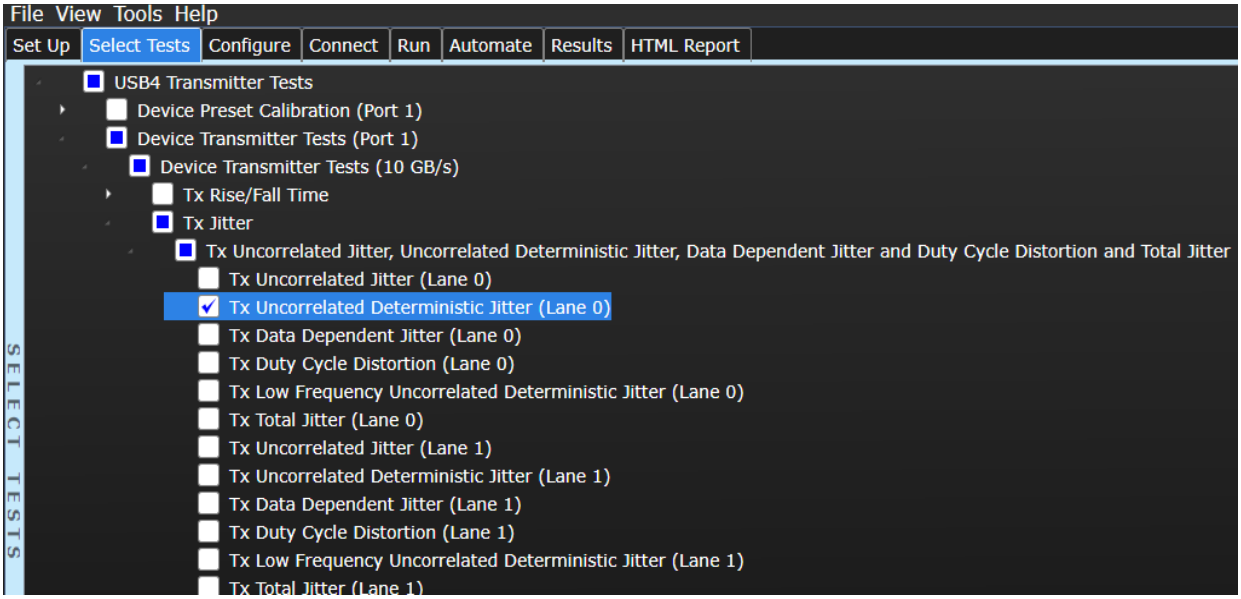


Figure 96 Selecting the Tx Uncorrelated Deterministic Jitter tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2 Perform measurements with:
   a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   b Oscilloscope with a minimum bandwidth of 16GHz
3 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Pattern length – Periodic
   c Jitter Separatio method must be suitable for cross-talk on the signal
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Evaluate 40 Mpts per channel when using 80 GSa/s. For higher sample rates, use memory depth in the same ratio to 40 Mpts
   f Referenced to 1E-13 statistics
4 Capture the UDJ result (same as BUJ over the Oscilloscope).
5 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If UDJ > 0.17 UI_{p-p}, the status of test is FAIL.

Test References

See

- USB4 Specification Version 2.00 (Table 3-5)

Tx Data Dependent Jitter

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Data Dependent Jitter Test is to confirm that the sum of Data Dependent Jitter (DDJ) of a USB4 device must be less than the maximum limit as per the specification.

Test Pass Requirement

Data Dependent Jitter (DDJ) $\leq$ 0.15 UI_{p-p} (Refer to Table 6 on page 83).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 86 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter, Data Dependent Jitter and Duty Cycle Distortion* are selected.

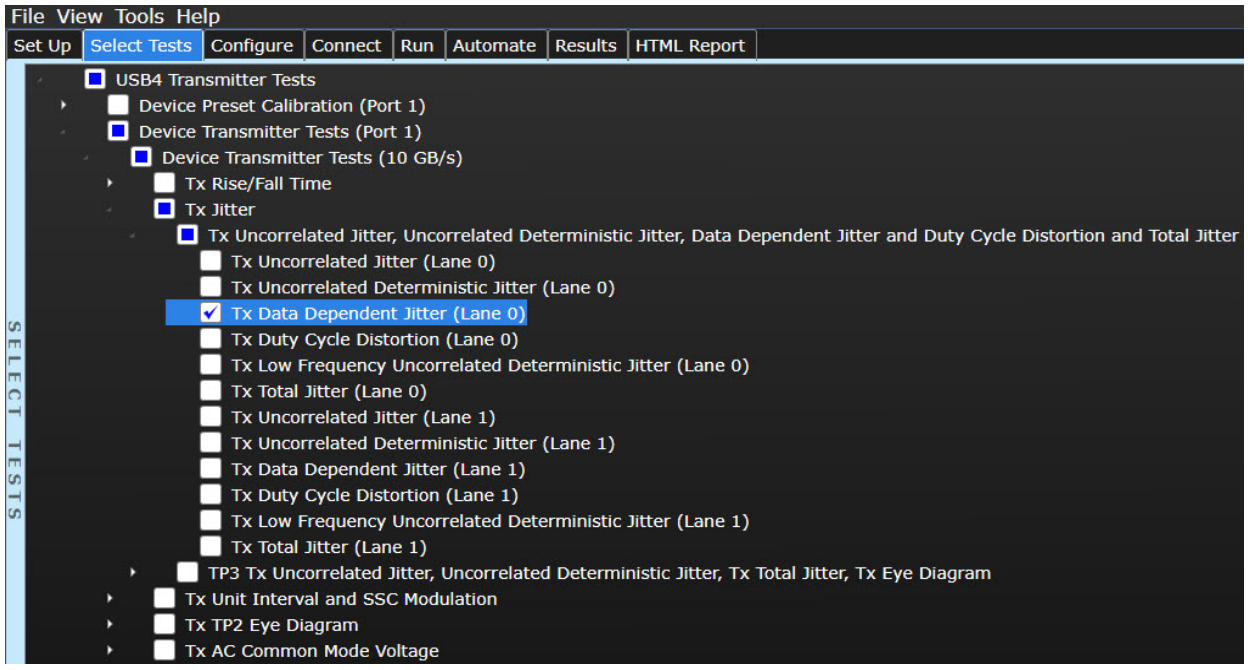


Figure 97 Selecting the Tx Data Dependent Jitter tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2 Perform measurements with:
   a Reference CDR based on the 2^{nd} order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   b Oscilloscope with a minimum bandwidth of 16 GHz
3 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Pattern length – Periodic
   c Jitter Separation method must be suitable for cross-talk on the signal
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Evaluate 40 Mpts per channel when using 80 GSa/s. For higher sample rates, use memory depth in the same ratio to 40 Mpts
   f Referenced to 1E-13 statistics
4 Capture the DDJ result (same as ISI over the Oscilloscope).
5 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If DDJ > 0.15 UI_{p-p}, the status of test is FAIL.

Test References

See

- *USB4 Specification Version 2.00 (Table 3-5)*

Tx Duty Cycle Distortion

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Duty Cycle Distortion Test is to confirm that the transmitter Deterministic Jitter associated by Duty-Cycle-Distortion Jitter falls within the limits of the specification.

Test Pass Requirement

Duty-Cycle-Distortion (DCD) ≤ 0.03 UIp-p (Refer to Table 6 on page 83).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 86 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter and Duty Cycle Distortion* are checked.

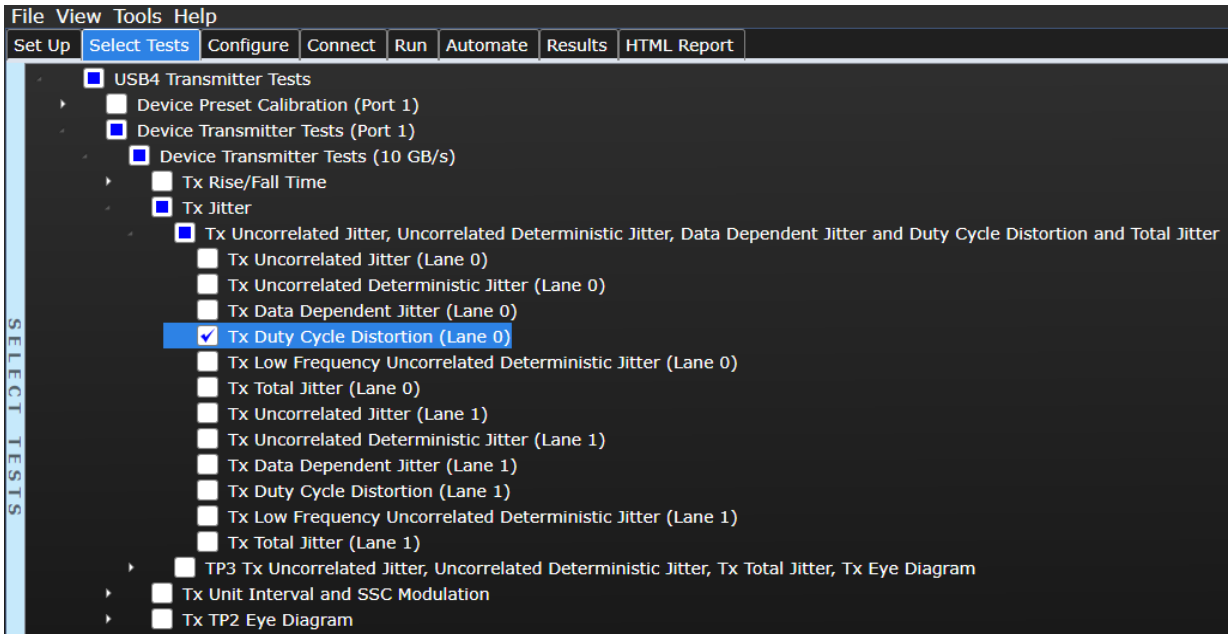


Figure 98 Selecting the Tx Duty Cycle Distortion tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2 Perform measurements with:
   a Reference CDR based on the 2^{nd} order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   b Oscilloscope with a minimum bandwidth of 16GHz
3 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Pattern length – Periodic
   c Jitter Separatio method must be suitable for cross-talk on the signal
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Evaluate 40 Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ratio to 40 Mpts.
4 Capture the DCD result.
5 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If DCD > 0.03UIp-p, the status of test is FAIL.

Test References

See

- *USB4 Specification Version 2.00 (Table 3-5)*

Tx Low Frequency Uncorrelated Deterministic Jitter

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Low Frequency Uncorrelated Deterministic Jitter Test is to confirm that the Low Frequency Uncorrelated Deterministic Jitter of the transmitter is within the limits of the specification.

Test Pass Requirement

Low Frequency Uncorrelated Deterministic Jitter (UDJ_LF) $\leq$ 0.04 UI_{p-p} (Refer to Table 6 on page 83).

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see Figure 86 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.
2. Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.
3. Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter, Data Dependent Jitter and Duty Cycle Distortion* are checked.

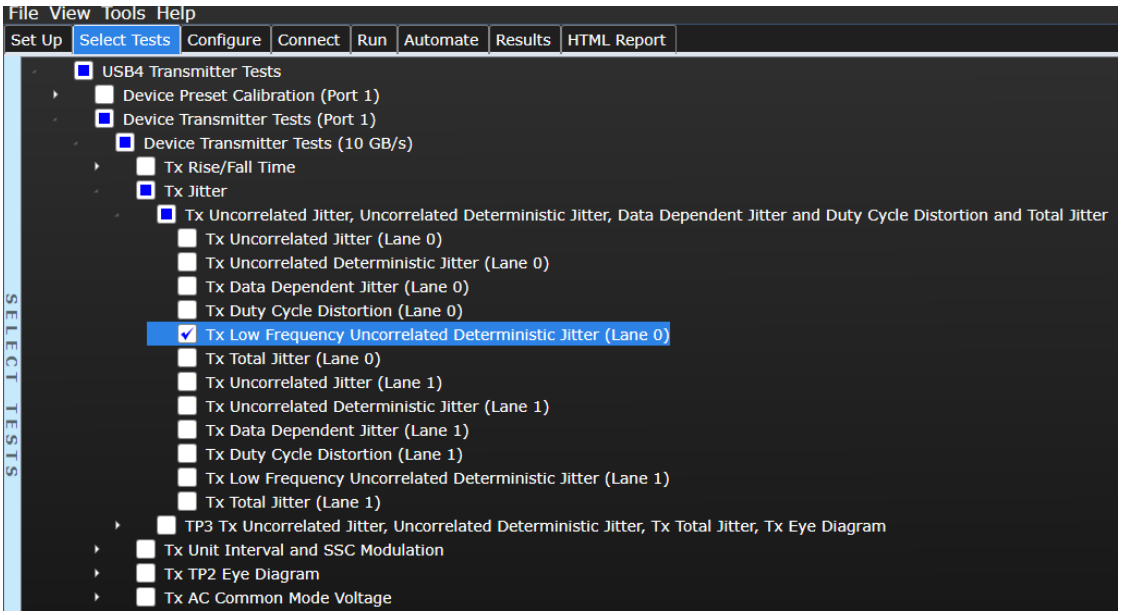


Figure 99 Selecting the Tx Low Frequency Uncorrelated Deterministic Jitter tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2 Perform measurements with:
   a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 0.5 MHz and damping factor of 0.94.
   b Apply 2^{nd} order Low-Pass-Filter with 3 dB cut-off at 2MHz; no average and no interpolation to be used
   c Oscilloscope with a minimum bandwidth of 16GHz
3 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Pattern length – Periodic
   c Jitter Separation method must be suitable for cross-talk on the signal
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Evaluate 40 Mpts per channel when using 80 GSa/s. For higher sample rates, use memory depth in the same ratio to 40 Mpts
4 Capture the UDJ_LF result.
5 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If UDJ_LF > 0.04 UI_{p-p}, the status of test is FAIL.

Test References

See

USB4 Specification Version 2.00 (Table 3-5)

Tx Total Jitter

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Total Jitter Test is to confirm that the Total Jitter of the transmitter is within the limits of the specification.

Total Jitter (TJ) is defined as the sum of all “deterministic” components plus 14.7 times the Random Jitter (RJ) RMS. 14.7 is the factor that accommodates a Bit Error Ratio value of $1x10^{-13}$.

Test Pass Requirement

Total Jitter (TJ) $\leq$ 0.38 UI_{p-p} (Refer to Table 6 on page 83).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 86 and for configuring the USB4 Test Application, see “Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to “Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Total Jitter* are checked.

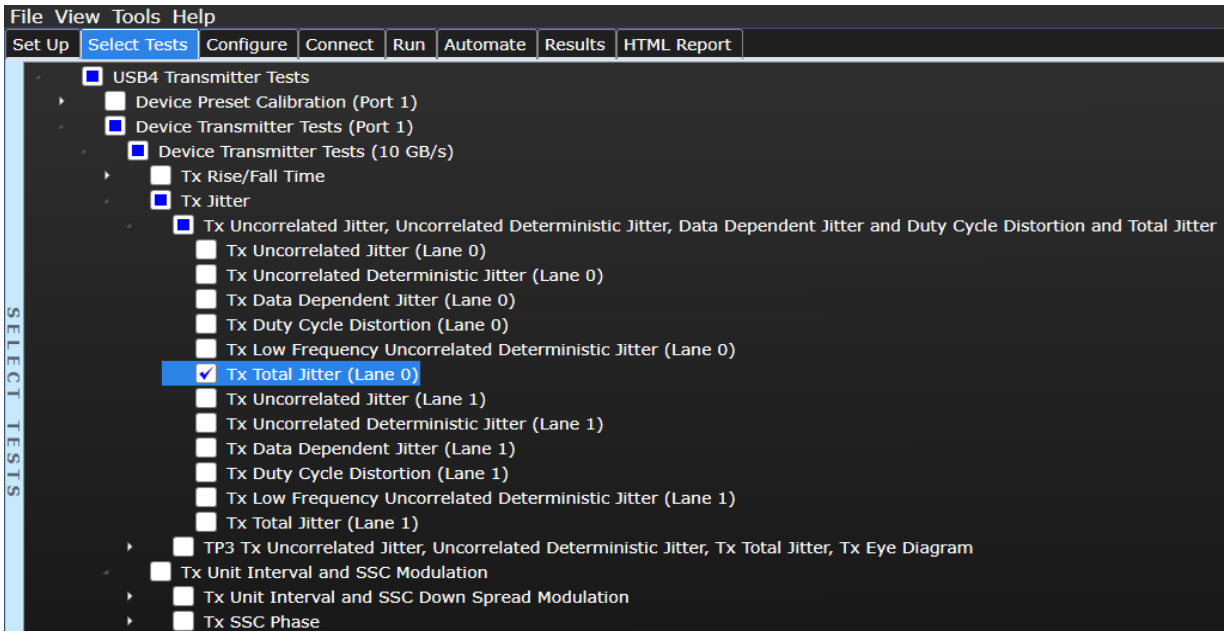


Figure 100 Selecting the Tx Total Jitter tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2 Perform measurements with:
   a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94
   b Oscilloscope with a minimum bandwidth of 16GHz
3 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Pattern length – Periodic
   c Jitter Separation method must be suitable for cross-talk on the signal
   d Evaluate 40 Mpts per channel when using 80 GSa/s. For higher sample rates, use memory depth in the same ratio to 40 Mpts
   e Adjust vertical scale such that the signal fits within the Oscilloscope's display.
   f Referenced to 1E-13 statistics.
4 Capture the values of Total Jitter (TJ) and Deterministic Jitter (DJ).
5 If TJ > 0.38 UI_{p-p}, perform the following steps:
   a Configure the DUT transmitter to output alternating square pattern of one 0's and one 1's on all lanes with SSC enabled. (The pattern is SQ2 instead of PRBS15).
   b Perform measurements with:
   - Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94
   - Oscilloscope with a minimum bandwidth of 16GHz

   c Capture the waveform and process it with the Digital Oscilloscope:
   - Sampling Rate $\geq$ 80 GSa/s
   - Pattern length – Periodic
   - Jitter Separation method must be suitable for cross-talk on the signal
   - Evaluate 40 Mpts per channel when using 80 GSa/s. For higher sample rates, use memory depth in the same ratio to 40 Mpts
   - Adjust vertical scale such that the signal fits within the Oscilloscope's display.
   - Referenced to 1E-13 statistics.

   d Capture the Random Jitter (RJ) result.
   e Calculate TJ using the equation:

$$TJ = DJ + 14.7 * RJ \text{ (DJ from \#4; PRBS15 and RJ from \#5d; SQ2)}$$

6 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If TJ > 0.38 UI_{p-p}, the status of test is FAIL.

Test References

See

USB4 Specification Version 2.00 (Table 3-5)

Tx Uncorrelated Jitter TP3

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Uncorrelated Jitter TP3 Test is to confirm that the Uncorrelated Jitter [Deterministic Jitter (DJ) and Random Jitter (RJ) components] at point TP3 of the transmitter is within the limits of the specification.

Test Pass Requirement

Uncorrelated Jitter (UJ_{TP3}) $\leq$ 0.31 UI_{p-p} (Refer to Table 7 on page 84).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 86 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter, Data Dependent Jitter and Duty Cycle Distortion* are checked.

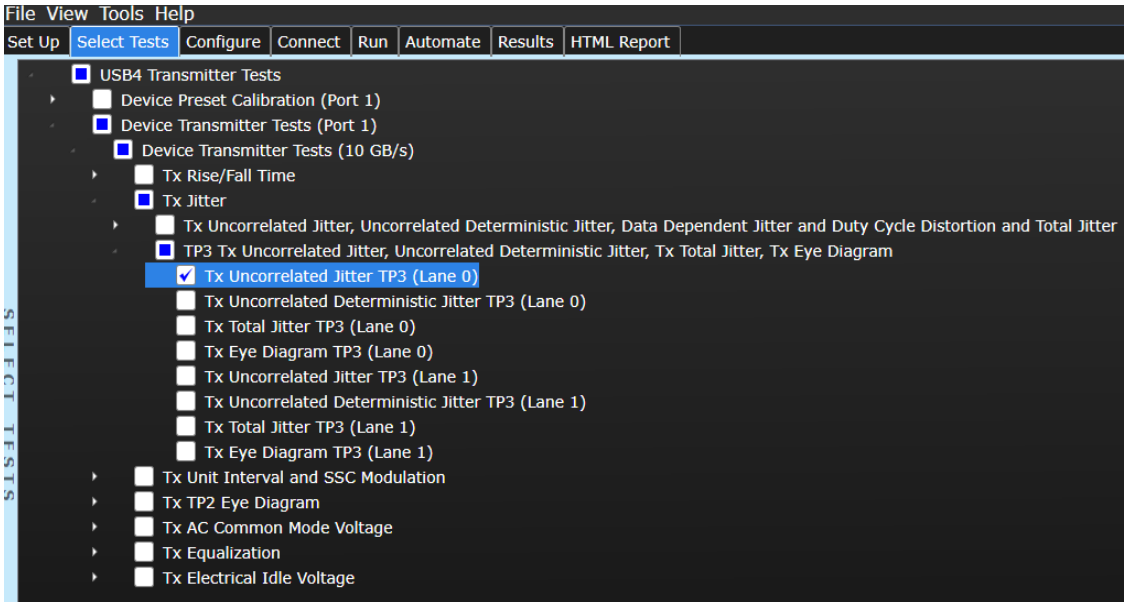


Figure 101 Selecting the Tx Uncorrelated Jitter TP3 tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2 Embed the Type-C cable in the Oscilloscope. For Gen 2 systems, use TP3_EQ embedding file *USB_2m.s4p*.
3 De-embed the cables from the test fixture to the Oscilloscope.
4 Perform measurements with:
   a Reference CDR based on the 2^{nd} order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   b Oscilloscope with a minimum bandwidth of 16GHz
5 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Pattern length – Periodic
   c Jitter Separation method must be suitable for cross-talk on the signal
   d Evaluate 40 Mpts per channel when using 80 GSa/s. For higher sample rates, use memory depth in the same ratio to 40 Mpts
   e Adjust vertical scale such that the signal fits within the Oscilloscope's display
   f Referenced to 1E-13 statistics
6 Capture the values of Total Jitter (TJ_{TP3}) and Data Deterministic Jitter (DDJ_{TP3}).
7 Calculate UJ_{TP3} using the equation:

$$UJ_{TP3} = TJ_{TP3} - DDJ_{TP3}$$

8 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If $UJ_{TP3} > 0.31\ UI_{p-p}$, the status of test is FAIL.

Test References

See

- USB4 Specification Version 2.00 (Table 3-6)

Tx Uncorrelated Deterministic Jitter TP3

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Uncorrelated Deterministic Jitter TP3 Test is to confirm that the Uncorrelated Deterministic Jitter at point TP3 of the transmitter is within the limits of the specification.

Test Pass Requirement

Deterministic Jitter that is uncorrelated to the transmitted data (UDJ_{TP3}) $\leq$ 0.17 UI_{p-p} (Refer to Table 7 on page 84).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 86 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter, Data Dependent Jitter and Duty Cycle Distortion* are checked.

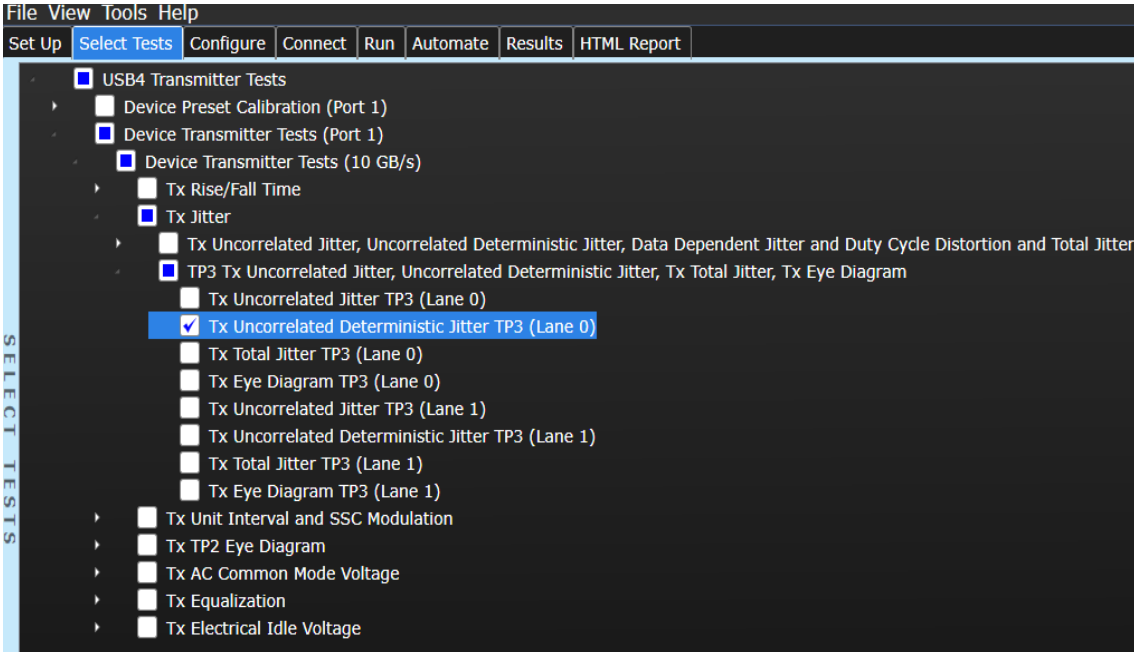


Figure 102 Selecting the Tx Uncorrelated Deterministic Jitter TP3 tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2 Embed the Type-C cable in the Oscilloscope. For Gen 2 systems, use TP3 embedding file *USB_2m.s4p*.
3 De-embed the cables from the test fixture to the Oscilloscope.
4 Perform measurements with:
   a Reference CDR based on the 2^{nd} order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   b Oscilloscope with a minimum bandwidth of 16GHz
5 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Pattern length – Periodic
   c Jitter Separation method must be suitable for cross-talk on the signal
   d Evaluate 40 Mpts per channel when using 80 GSa/s. For higher sample rates, use memory depth in the same ratio to 40 Mpts
   e Adjust vertical scale such that the signal fits within the Oscilloscope's display
6 Capture the values of Total Jitter (TJ_{TP3}) and Data Deterministic Jitter (DDJ_{TP3}).
7 Capture the UDJ_{TP3} result (same as BUJ over the Oscilloscope).
8 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If $UDJ_{TP3} > 0.17\ UI_{p-p}$, the status of test is FAIL.

Test References

See

USB4 Specification Version 2.00 (Table 3-6)

Tx Total Jitter TP3

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Total Jitter TP3 Test is to confirm that the Total Jitter at point TP3 of the transmitter is within the limits of the specification.

Total Jitter (TJ) is defined as the sum of all “deterministic” components plus 14.7 times the Random Jitter (RJ) RMS. 14.7 is the factor that accommodates a Bit Error Ratio value of $1x10^{-13}$.

Test Pass Requirement

Total Jitter (TJ_{TP3}) $\leq$ 0.60 UI_{p-p} (Refer to Table 7 on page 84).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 86 and for configuring the USB4 Test Application, see “Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to “Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Total Jitter* are checked.

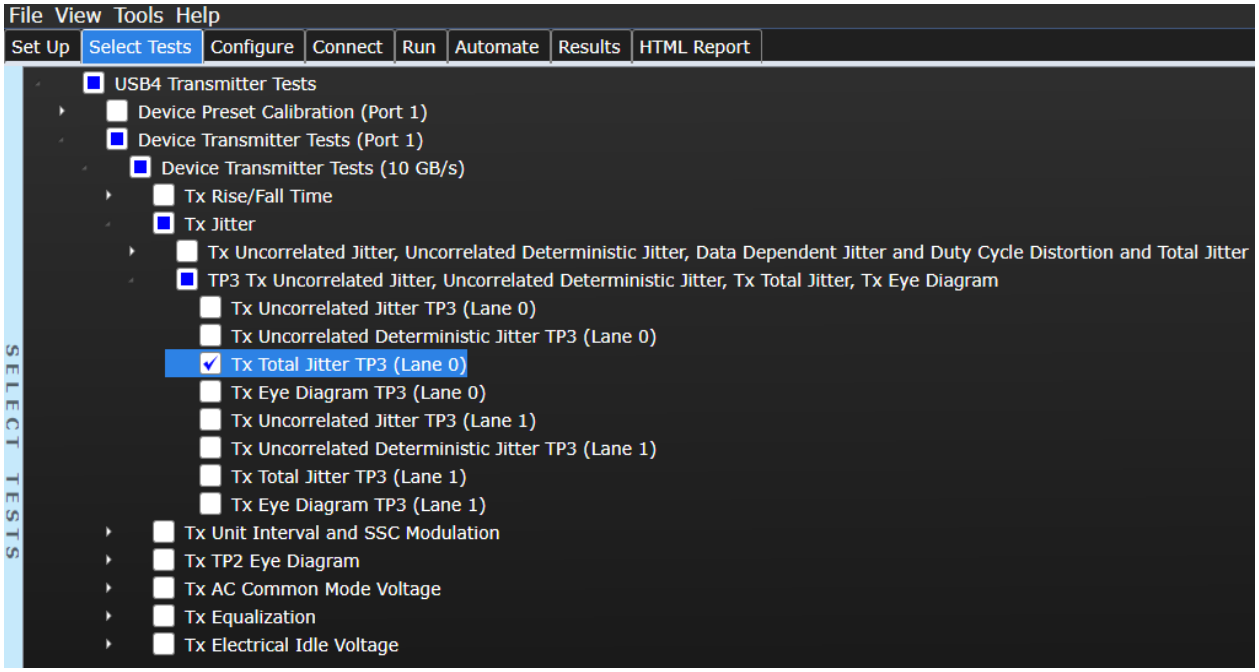


Figure 103 Selecting the Tx Total Jitter TP3 tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2 Embed the Type-C cable in the Oscilloscope. For Gen 2 systems, use TP3_EQ embedding file *USB_2m.s4p*.
3 De-embed the cables from the test fixture to the Oscilloscope.
4 Perform measurements with:
   a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   b Oscilloscope with a minimum bandwidth of 16GHz
5 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Pattern length – Periodic
   c Jitter Separation method must be suitable for cross-talk on the signal
   d Evaluate 40 Mpts per channel when using 80 GSa/s. For higher sample rates, use memory depth in the same ratio to 40 Mpts
   e Adjust vertical scale such that the signal fits within the Oscilloscope's display
   f Referenced to 1E-13 statistics
6 Capture the values of Total Jitter (TJ_{TP3}) and Deterministic Jitter (DJ_{TP3}).
7 If $TJ_{TP3} > 0.60\ UI_{p-p}$, perform the following steps:
   a Configure the DUT transmitter to output alternating square pattern of one 0's and one 1's on all lanes with SSC enabled. (The pattern is SQ2 instead of PRBS15).
   b Perform measurements with:
   - Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94
   - Oscilloscope with a minimum bandwidth of 16GHz

   c Capture the waveform and process it with the Digital Oscilloscope:
   - Sampling Rate $\geq$ 80 GSa/s
   - Pattern length – Periodic
   - Jitter Separation method must be suitable for cross-talk on the signal
   - Evaluate 40 Mpts per channel when using 80 GSa/s. For higher sample rates, use memory depth in the same ratio to 40 Mpts
   - Adjust vertical scale such that the signal fits within the Oscilloscope's display.
   - Referenced to 1E-13 statistics.

   d Capture the Random Jitter (RJ_{TP3}) result.
   e Calculate TJ_{TP3} using the equation:

$$TJ_{TP3} = DJ_{TP3} + 14.7 * RJ_{TP3}$$ (DJ_{TP3} from #7; PRBS15 and RJ_{TP3} from #8d; SQ2)

8 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If $TJ_{TP3} > 0.60\ UI_{p-p}$, the status of test is FAIL.

Test References

See

USB4 Specification Version 2.00 (Table 3-7)

Tx Eye Diagram TP3

Test Overview

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

The objective of the Tx Eye Diagram TP3 Test is to confirm that the differential signal on each USB differential lane has an eye opening that meets or exceeds the limits for eye opening in the specification.

Test Pass Requirement

The eye diagram at TP3 should meet the conditions depicted in Figure 104.

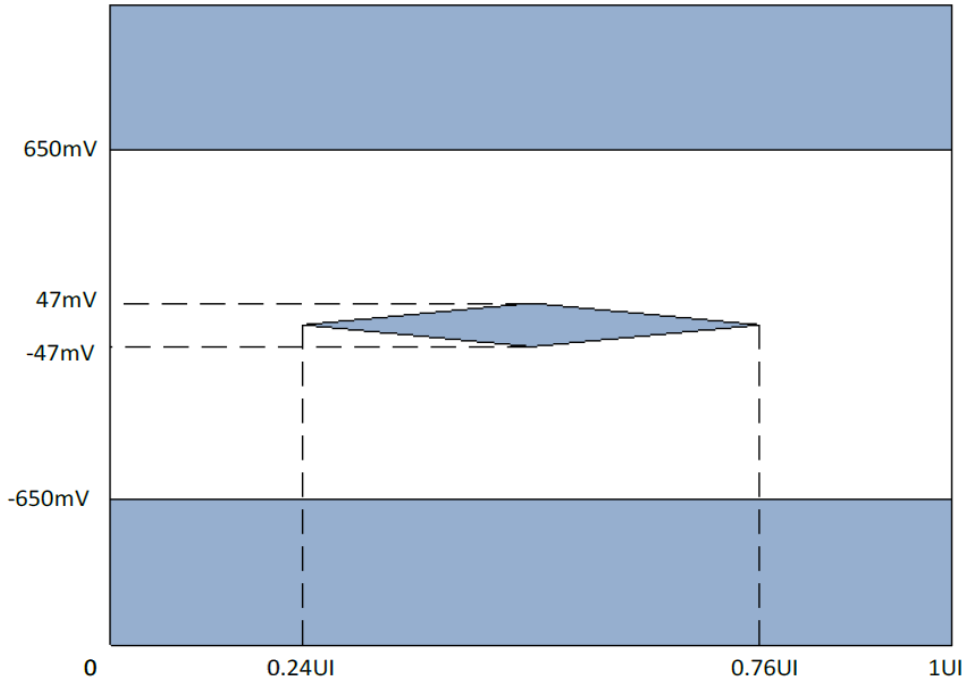


Figure 104 Pass Condition for Tx Eye Diagram TP3 Tests

(Refer to Table 7 on page 84 and Figure 104 on page 216).

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see "Transmitter TP2/TP3 Test Setup" on page 180 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.
2. Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.
3. Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Eye Diagram* are checked.

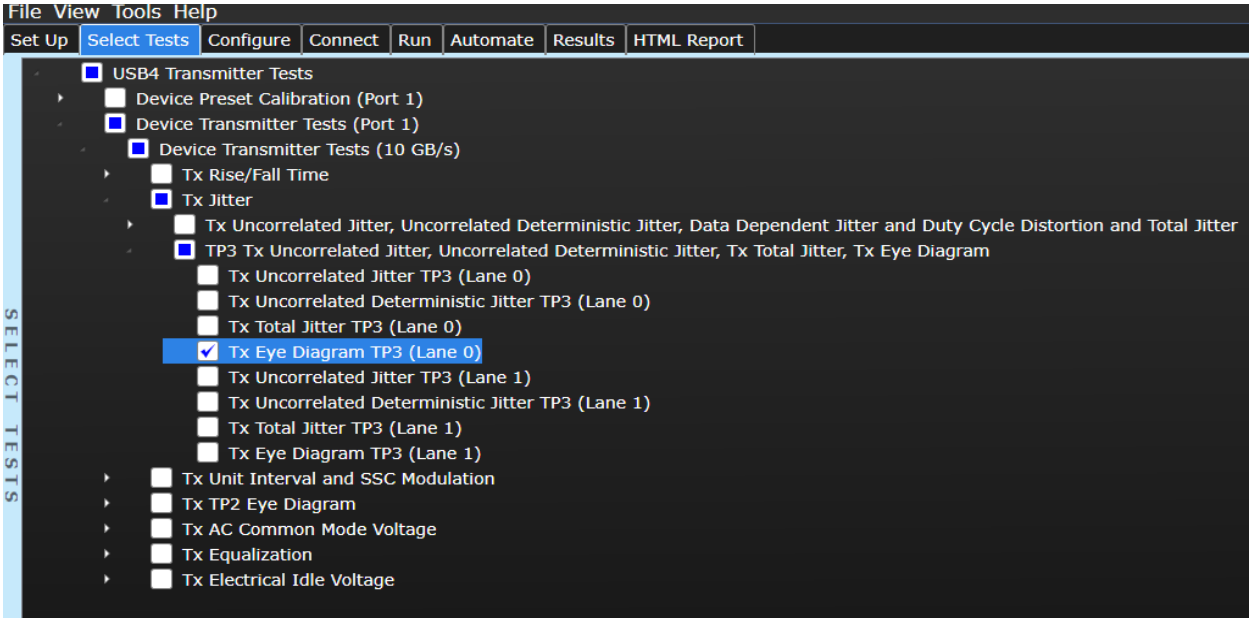


Figure 105 Selecting the Tx Eye Diagram TP3 tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.

2 Embed the Type-C cable in the Oscilloscope. For Gen 2 systems, use TP3 embedding file *USB_2m.s4p*.

3 De-embed the cables from the test fixture to the Oscilloscope.

4 Perform measurements with:

a Change from no interpolation to X16 a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and X16 interpolation to be used.

b Oscilloscope with a minimum bandwidth of 16GHz

5 Capture the waveform and process it with the Digital Oscilloscope:

a Sampling Rate $\geq$ 80 GSa/s

b Adjust vertical and horizontal scale such that the signal fits within the Oscilloscope's display

c Accumulate at 1E6 UI

6 Compare the data eye to the TP3 eye diagram mask. Check for conditions described in the section "Expected / Observable Results".

7 Repeat the test for the remaining USB lanes.

Expected / Observable Results

i If any part of the waveform exceeds either the high or low maximum voltage (+/-1000mV), the status of the test is FAIL.

ii If any part of the waveform hits the mask, the status of the test is FAIL.

Test References

See

- USB4 Specification Version 2.00 (Table 3-6)

Tx Minimum Unit Interval, Min/Max

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Unit Interval Test is to confirm that the data rate, under all conditions, does not exceed the minimum or maximum limits of the specification.

Test Pass Requirement

Tx Minimum Unit Interval Min

Minimum Unit Interval, Min (Device, 10 Gb/s) >= 99.9700 ps

Tx Minimum Unit Intreval Max

Minimum Unit Interval, Max (Device, 10 Gb/s) <= 100.0300 ps

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see Figure 86 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.
2. Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.
3. Under the **Select Tests** tab of the USB4 Test Application, ensure that the tests under the test group *Tx Unit Interval and SSC Down Spread Modulation* are checked.

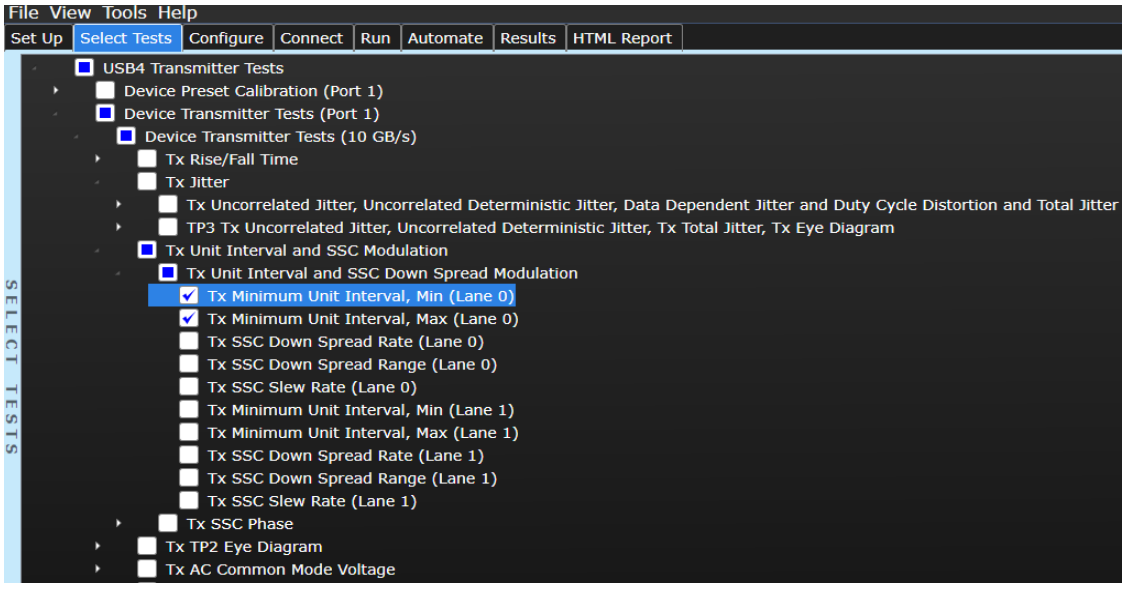


Figure 106 Selecting the Tx Unit Interval tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ratio to 27Mpts
   c No CDR, no average and no interpolation to be used
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Oscilloscope must have a minimum bandwidth of 16GHz
3 Calculate UI dynamically using a uniform moving average filter procedure with a window size of 3000 symbols.
4 Measure the values of both UI_{MAX} and UI_{MIN}.
5 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If $UI_{MAX} > 100.0300$ ps, the status of test is FAIL.

If $UI_{MIN} < 99.9700$ ps, the status of test is FAIL.

Test References

See

- USB4 Specification Version 2.00 (Table 3-5)

Tx SSC Down Spread Rate

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx SSC Down Spread Rate Test is to confirm that the Link clock down-spreading modulation rate is within the limits of the specification.

Test Pass Requirement

30.00 kHz $\leq$ SSC_Down_Spread_Rate $\leq$ 33.00 kHz (Refer to Table 3 on page 74).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 86 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Unit Interval and SSC Down Spread Modulation* are checked.

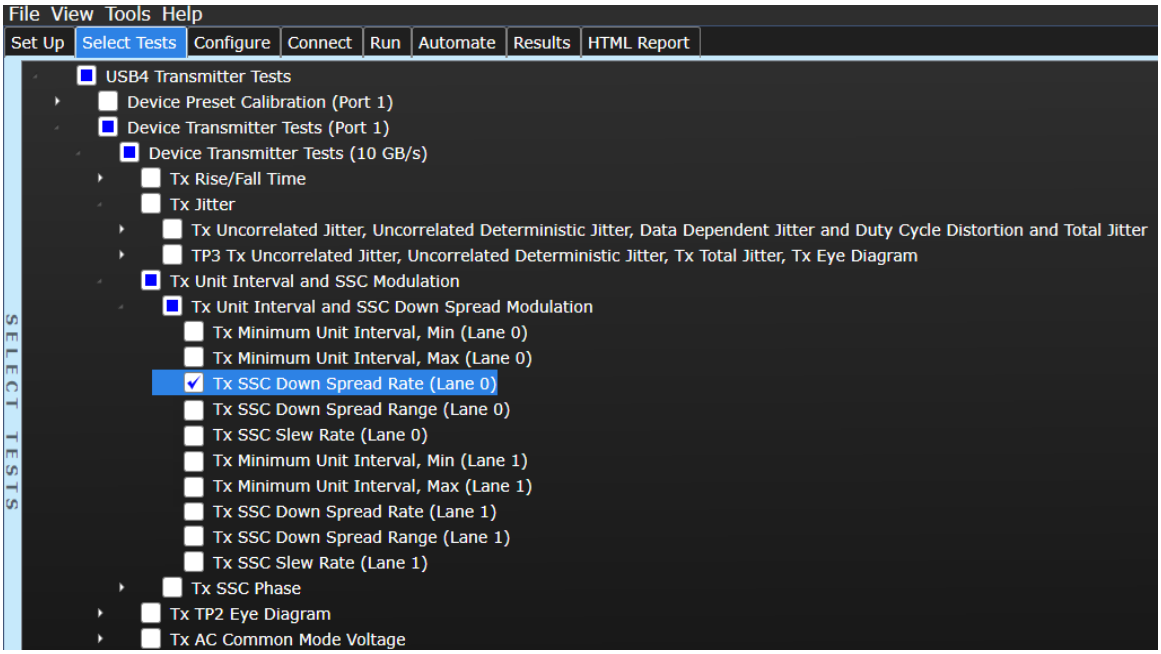


Figure 107 Selecting the Tx SSC Down Spread Rate tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ratio to 27Mpts
   c No CDR, no average and no interpolation to be used
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Oscilloscope must have a minimum bandwidth of 16GHz
3 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If 30.00 kHz > SSC_Down_Spread_Rate > 33.00 kHz, the status of test is FAIL.

Test References

See

- *USB4 Specification Version 2.00 (Table 3-2)*

Tx SSC Down Spread Range

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx SSC Down Spread Range Test is to confirm that the data down spreading is within the limits of the specification.

Test Pass Requirement

0.4% ≤ SSC_Down_Spread_Range ≤ 0.5% (Refer to Table 3 on page 74).

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see Figure 86 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.
2. Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.
3. Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Unit Interval and SSC Down Spread Modulation* are checked.

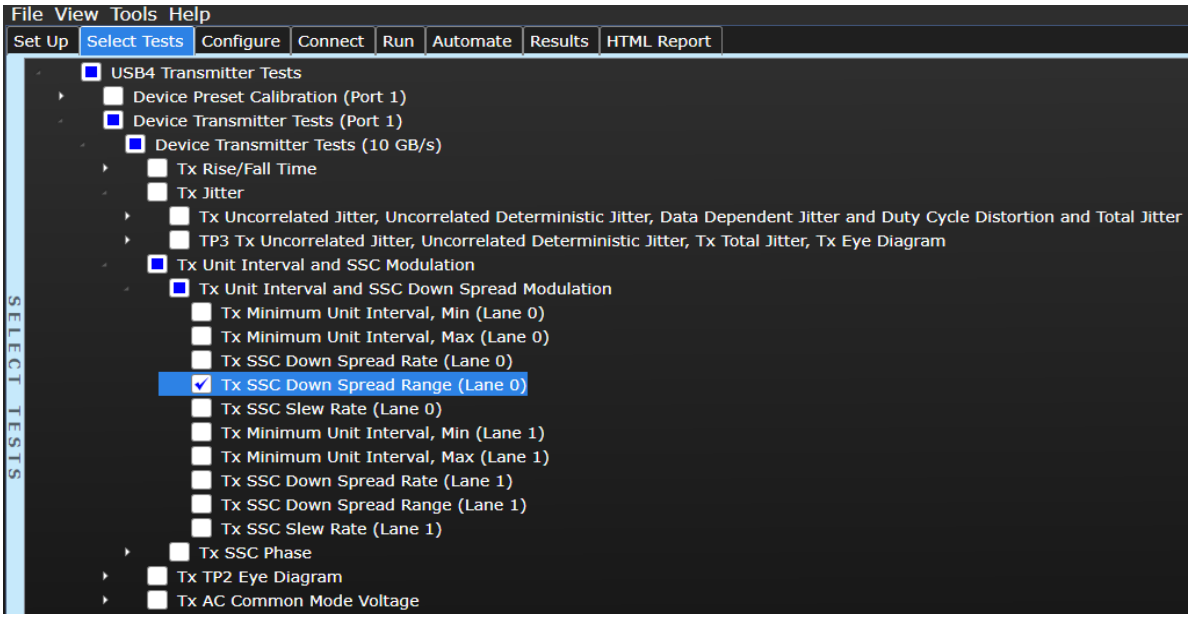


Figure 108 Selecting the Tx SSC Down Spread Range tests

Test Procedure

1 Run the "Tx Eye Diagram TP3" Test as a prerequisite to obtain UI_{MAX} and UI_{MIN}.
2 Use the obtained value of UI_{MAX} and UI_{MIN} to calculate the Range percentage:

$$\text{Maximum Deviation} = 100*\{[10G - (1 / UI_{MAX})] / 10G\}$$

$$\text{Minimum Deviation} = 100*\{[10G - (1 / UI_{MIN})] / 10G\}$$

3 Calculate SSC Down Spread Range using the equation:

$$\text{Maximum Deviation - Minimum Deviation}$$

4 Repeat the test for all remaining USB lanes.

Expected / Observable Results

If SSC_Down_Spread_Range > 0.5% or SSC_Down_Spread_Range < 0.4%, the status of test is FAIL.

Test References

See

USB4 Specification Version 2.00 (Table 3-2)

Tx SSC Slew Rate

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx SSC Slew Rate Test is to confirm that the SSC Slew Rate is within the limits of the specification.

Test Pass Requirement

SSC_Slew_Rate $\leq$ 1250 ppm/µs (Refer to Table 3 on page 74).

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see Figure 86 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.
2. Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.
3. Under the **Select Tests** tab of the USB4 Test Application, ensure that the tests under the test group *Tx Unit Interval and SSC Down Spread Modulation* are checked.

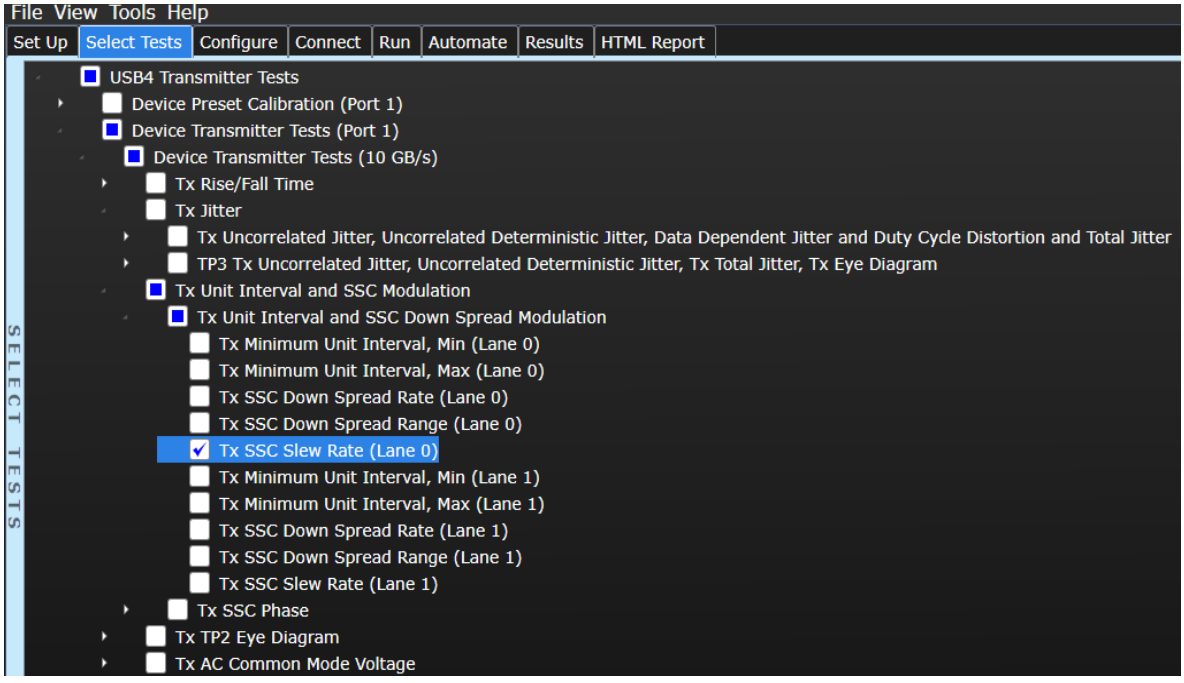


Figure 109 Selecting the Tx SSC Slew Rate tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2 Capture the waveform and post process it with an appropriate software:
   a Sampling Rate $\geq$ 80 GSa/s
   b Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ratio to 27Mpts
   c No CDR, no average and no interpolation to be used
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Extract SSC slew rate from the transmitted signal over measurement intervals of 0.5µs
   f Extract SSC slew rate from the phase information after applying a 2^{nd} order Low-Pass-Filter with 3 dB cut-off at 5 MHz.
   g Oscilloscope must have a minimum bandwidth of 16GHz
3 SSC_Slew_Rate is measured as the SSC frequency deviation over time while valid data is being transmitted in which 1E-12 bit error rate is required without assuming forward error correction.
4 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If SSC_Slew_Rate > 1250 ppm/µs, the status of test is FAIL.

Test References

See

USB4 Specification Version 2.00 (Table 3-2)

Tx SSC Phase Deviation

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx SSC Phase Deviation Test is to confirm that the SSC Phase Deviation is within the limits of the specification.

Test Pass Requirement

2.50 ns p-p $\leq$ SSC_Phase_Deviation $\leq$ 22.00 ns p-p (Refer to Table 3 on page 74).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 86 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx SSC Phase* are checked.

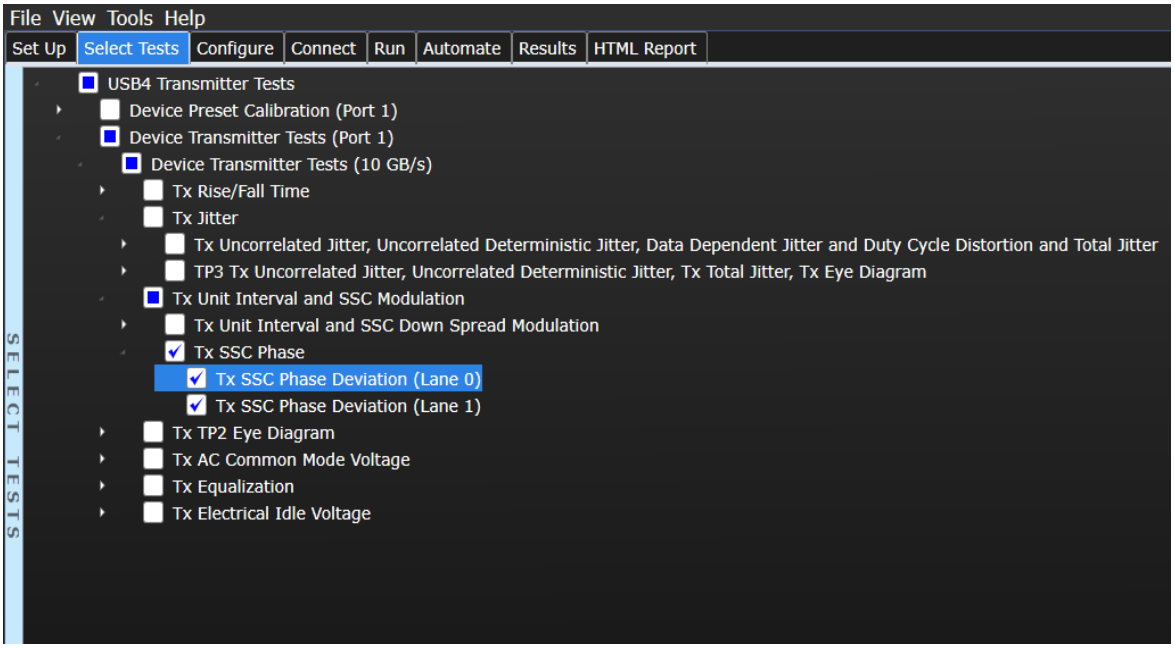


Figure 110 Selecting the Tx SSC Phase Deviation tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2 Capture the waveform and process it with the Digital Oscilloscope's software:
   a Sampling Rate $\geq$ 80 GSa/s
   b Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ratio to 27Mpts
   c No CDR, no average and no interpolation to be used
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Oscilloscope must have a minimum bandwidth of 16GHz
3 Extract the SSC Phase Deviation from the transmitted signal.
4 Extract the SSC Phase Deviation from the phase jitter after applying a 2^{nd} order low-pass filter with 3dB point at 5 MHz.
5 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If 2.50 ns p-p > SSC_Phase_Deviation > 22.00 ns p-p the status of test is FAIL.

Test References

See

- USB4 Specification Version 2.00 (Table 3-2)

Tx Eye Diagram

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Eye Diagram Test is to confirm that the differential signal on each USB differential lane has an eye opening that meets or exceeds the limits for eye opening in the specification.

Test Pass Requirement

The eye diagram should meet the conditions depicted in Figure 111.

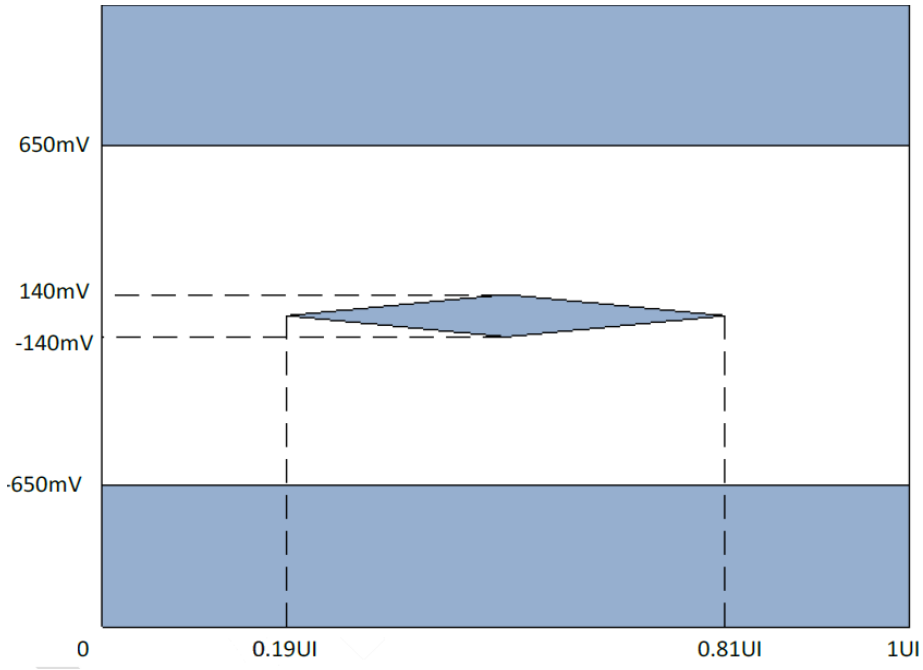


Figure 111 Pass Condition for Tx Eye Diagram Tests

(Refer to Table 6 on page 83 and Figure 111 on page 229)

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter TP2/TP3 Test Setup" on page 180 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Eye Diagram* are checked.

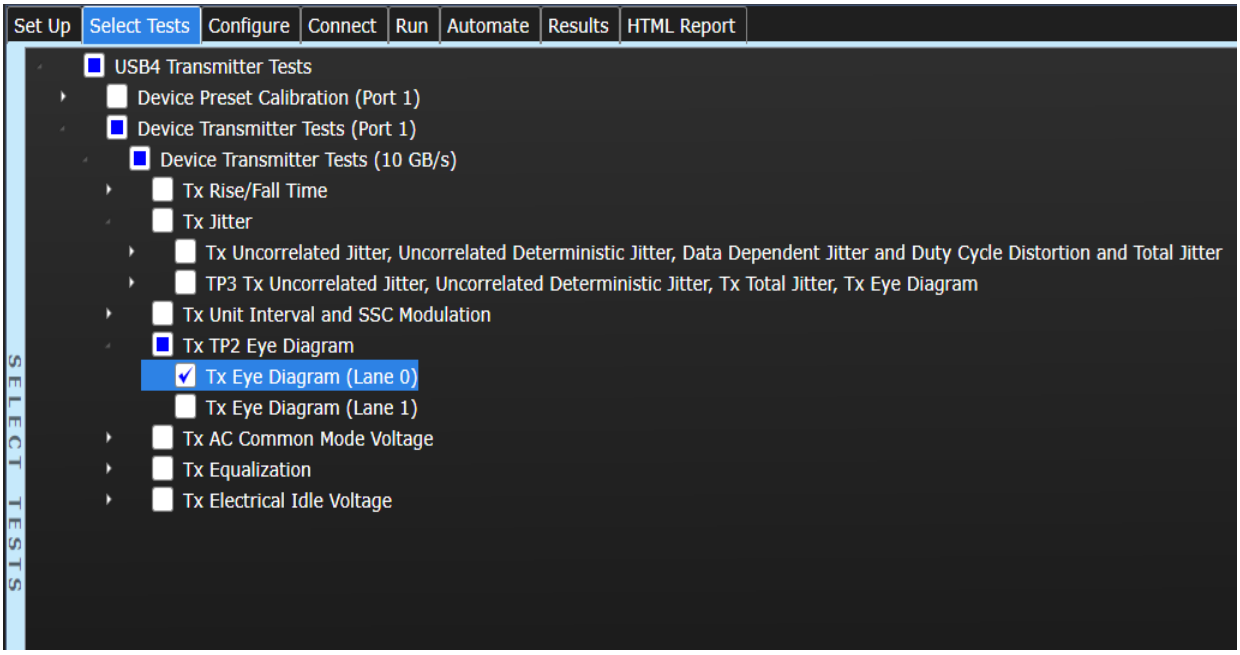


Figure 112 Selecting the Tx Eye Diagram tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2 Perform measurements with:
   a Change from no interpolation to X16 a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and X16 interpolation to be used.
   b Oscilloscope with a minimum bandwidth of 16GHz
3 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Adjust vertical scale such that the signal fits within the Oscilloscope's display
   c Measured at 1E6 UI
4 Compare the data eye to the TP1 eye diagram mask. Check for conditions described in the section "Expected / Observable Results".
5 Repeat the test for the remaining USB lanes.

Expected / Observable Results

i If any part of the waveform exceeds either the inner or outer height voltage (+/- 700mV), the status of the test is FAIL.
ii If any part of the waveform hits the mask, the status of the test is FAIL.

Test References

See

- Universal Serial Bus 4 (USB Type-C) Specification Version 1.00 (Table 5-6)

Tx AC Common Mode Voltage

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx AC Common Mode Voltage Test is to confirm that the transmitter common mode on the USB differential signals is within the limits of the specification.

Test Pass Requirement

TX AC Common Mode Voltage $\leq$ 100 mV_{p-p} (Refer to Table 6 on page 83).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 86 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx AC Common Mode Voltage* are checked.

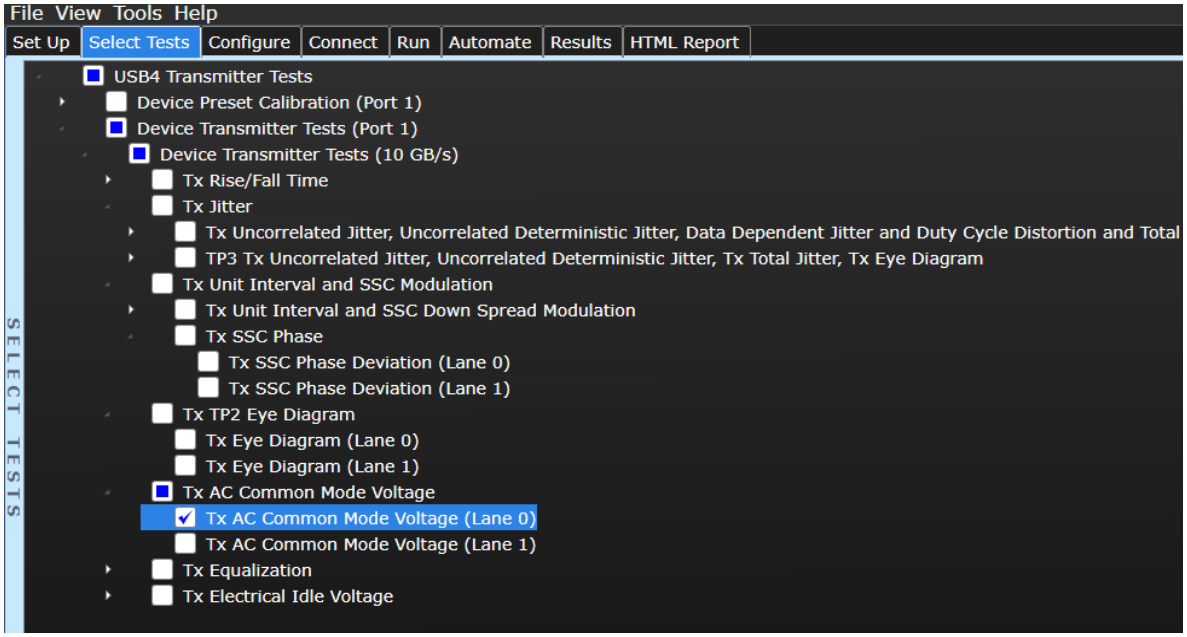


Figure 113 Selecting the Tx AC Common Mode Voltage tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ratio to 27Mpts
   c No CDR, no average and no interpolation to be used
   d Oscilloscope must have a minimum bandwidth of 16GHz
3 Calculate the AC Common Mode Voltage (V_{AC-CM}) using the equation:

$$V_{AC-CM} = (V_{TX-P} + V_{TX-N}) / 2$$

4 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If $V_{AC-CM} > 100mV_{p-p}$, the status of test is FAIL.

Test References

See

USB4 Specification Version 2.00 (Table 3-5)

Tx Equalization Tests

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Equalization Tests is to confirm that the transmitter equalization is within the limits of the specification. The Tx Equalization Tests are further divided into three tests, namely:

- Tx Equalization Preshoot
- Tx Equalization Deemphasis
- Tx Swing Preset 15

Test Pass Requirement

Transmitter Swing: 3.5 ± 1dB (for preset 15 only)

Preshoot, De-Emphasis: ± 1dB for the following presets:

Table 11 Transmitter Equalization Presets

Preset Number	Pre-Shoot	De-Emphasis	Informative Filter Coefficients		
			C_{-1}	C_0	C_1
0	0	0	0	1	0
1	0	-1.9	0	0.90	-0.10
2	0	-3.6	0	0.83	-0.17
3	0	-5.0	0	0.78	-0.22
4	0	-8.4	0	0.69	-0.31
5	0.9	0	-0.05	0.95	0
6	1.1	-1.9	-0.05	0.86	-0.09
7	1.4	-3.8	-0.05	0.79	-0.16
8	1.7	-5.8	-0.05	0.73	-0.22
9	2.1	-8.0	-0.05	0.68	-0.27
10	1.7	0	-0.09	0.91	0
11	2.2	-2.2	-0.09	0.82	-0.09
12	2.5	-3.6	-0.09	0.77	-0.14
13	3.4	-6.7	-0.09	0.69	-0.22
14	3.6	0	-0.17	0.83	0
15	1.7	-1.7	-0.05	0.55	-0.05

(Refer to Table 5 on page 81).

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see Figure 86 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.
2. Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.
3. Under the **Select Tests** tab of the USB4 Test Application, ensure that the tests under the test group *Tx Equalization* are checked.

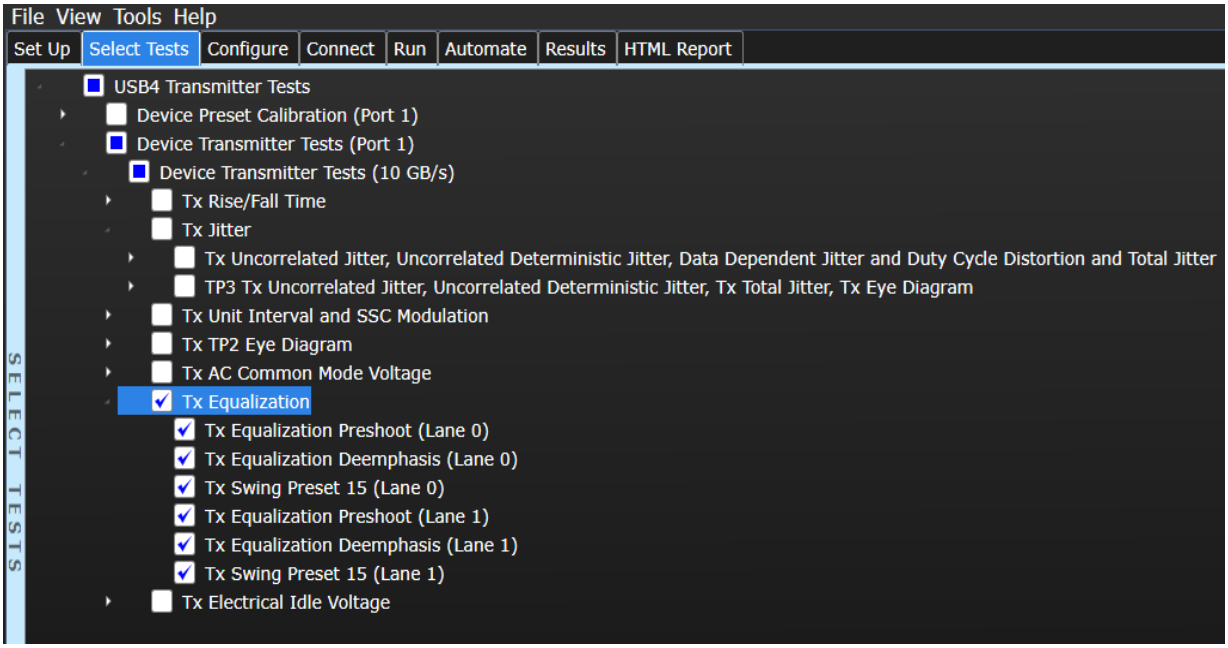


Figure 114 Selecting the Tx Equalization tests

4 Under the **Configure** tab of the Test Application, select **ALL** for the configuration Variable “Tx Equalization” to run the tests for preset numbers P0 to P15.

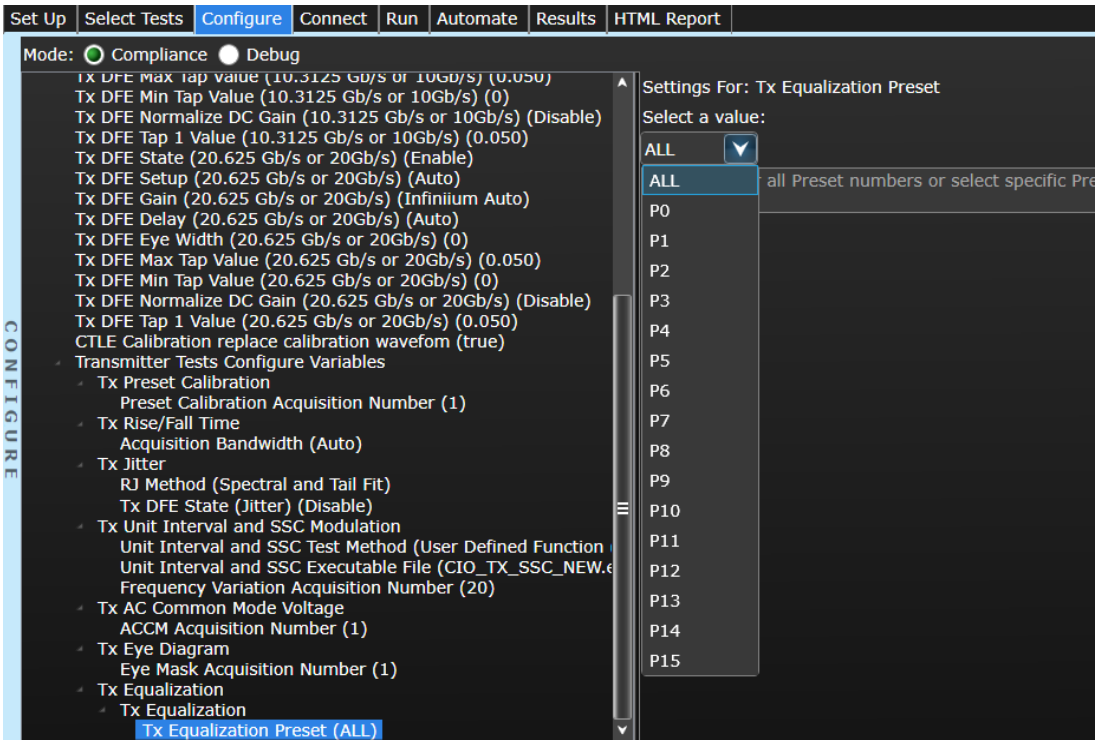


Figure 115 Configuring Tx Equalization Preset Variable

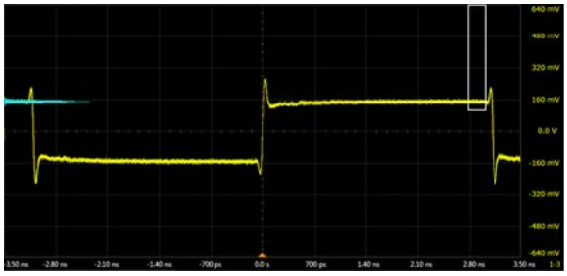
Test Procedure

1 Set Preset 0 (P0).

2 Configure the DUT transmitter to output alternating square pattern of 64 0’s and 64 1’s on all lanes with SSC enabled along with both pre-shoot and de-emphasis enabled.

3 Adjust vertical scale such that the signal fits within the Oscilloscope’s display.

4 Average one cycle using 150 cycles; no CDR and no interpolation to be used. Oscilloscope must have a minimum bandwidth of 16GHz.



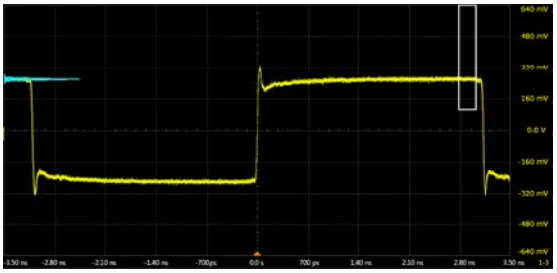
5 Measure differential amplitude voltage (V_1) for bits 57 to 62 using the equation:

$$V_1 = [|V_{bits(57\text{-}62)} \text{ (64 bits of 1's)} - V_{bits(57\text{-}62)} \text{ (64 bits of 0's)}|]$$

6 Configure the DUT transmitter to output alternating square pattern of 64 0’s and 64 1’s on all lanes with SSC enabled along with de-emphasis enabled but no pre-shoot.

7 Adjust vertical scale such that the signal fits within the Oscilloscope's display.

8 Average one cycle using 150 cycles; no CDR and no interpolation to be used. Oscilloscope must have a minimum bandwidth of 16GHz.



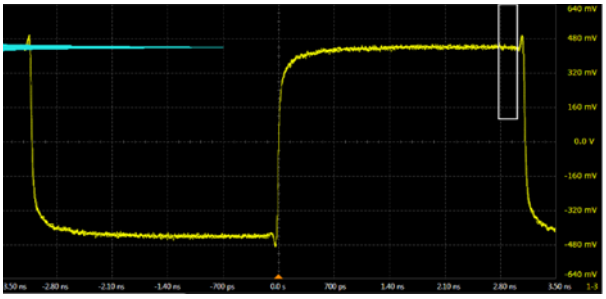
9 Measure differential amplitude voltage (V_2) for bits 57 to 62 using the equation:

$$V_2 = [|V_{bits(57-62)} \text{ (64 bits of 1's)} - V_{bits(57-62)} \text{ (64 bits of 0's)}|]$$

10 Configure the DUT transmitter to output alternating square pattern of 64 0's and 64 1's on all lanes with SSC enabled along with pre-shoot enabled but no de-emphasis.

11 Adjust vertical scale such that the signal fits within the Oscilloscope's display.

12 Average one cycle using 150 cycles; no CDR and no interpolation to be used. Oscilloscope must have a minimum bandwidth of 16GHz.



13 Measure differential amplitude voltage (V_3) for bits 57 to 62 using the equation:

$$V_3 = [|V_{bits(57-62)} \text{ (64 bits of 1's)} - V_{bits(57-62)} \text{ (64 bits of 0's)}|]$$

$$\text{Set Pre-Shoot to be } 20 * \log_{10} [V_2/V_1]$$

$$\text{Set De-Emphasis to be } 20 * \log_{10} [V_1/V_3]$$

14 Repeat steps 2 to 10 for all Presets defined in Table 11.

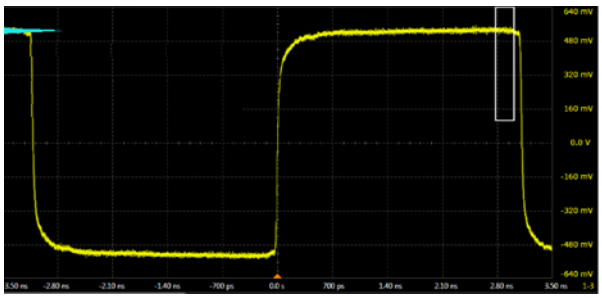
15 Check for PASS/FAIL conditions for both Pre-shoot and De-emphasis.

16 Set the DUT to Preset 0 (P0).

17 Configure the DUT transmitter to output alternating square pattern of 64 0's and 64 1's on all lanes with SSC enabled but with both pre-shoot and de-emphasis disabled.

18 Adjust vertical scale such that the signal fits within the Oscilloscope's display.

19 Average one cycle using 150 cycles; no CDR and no interpolation to be used. Oscilloscope must have a minimum bandwidth of 16GHz.



20 Measure differential amplitude voltage (V_0) for bits 57 to 62 using the equation:

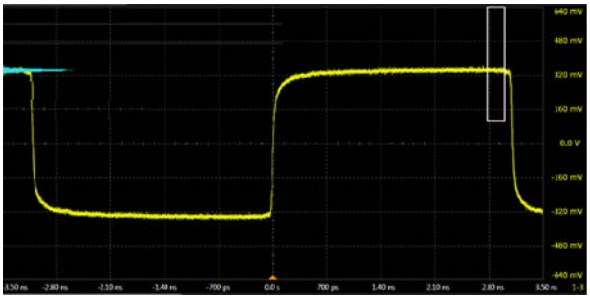
$$V_0 = [|V_{bits(57\text{-}62)} \text{ (64 bits of 1's)} - V_{bits(57\text{-}62)} \text{ (64 bits of 0's)}|]$$

21 Set the DUT to Preset 15 (P15).

22 Configure the DUT transmitter to output alternating square pattern of 64 0's and 64 1's on all lanes with SSC enabled but with both pre-shoot and de-emphasis disabled.

23 Adjust vertical scale such that the signal fits within the Oscilloscope's display

24 Average one cycle using 150 cycles; no CDR and no interpolation to be used. Oscilloscope must have a minimum bandwidth of 16GHz.



25 Measure differential amplitude voltage (V_{15}) for bits 57 to 62 using the equation:

$$V_{15} = [|V_{bits(57\text{-}62)} \text{ (64 bits of 1's)} - V_{bits(57\text{-}62)} \text{ (64 bits of 0's)}|]$$

Set Swing to be $20 * \log_{10} [V_0/V_{15}]$

26 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If the Pre-Shoot for a particular Preset number is not within ± 1dB of the matching value in Table 11, the status of test is FAIL.

If the De-Emphasis for a particular Preset number is not within ± 1dB of the matching value in Table 11, the status of test is FAIL.

If Swing < 2.5 dB or Swing > 4.5 dB, the status of test is FAIL.

Test References

See

- USB4 Specification Version 2.00 *(Table 3-4)*

Tx Electrical Idle Voltage Test

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Electrical Idle Voltage Test is to confirm that the transmitter peak voltage during electrical idle do not exceed the limits of the specification.

Test Pass Requirement

Tx Electrical Idle Voltage ≤ 20 mV_{p-p}

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 86 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group **Tx Electrical Idle Voltage** are selected.

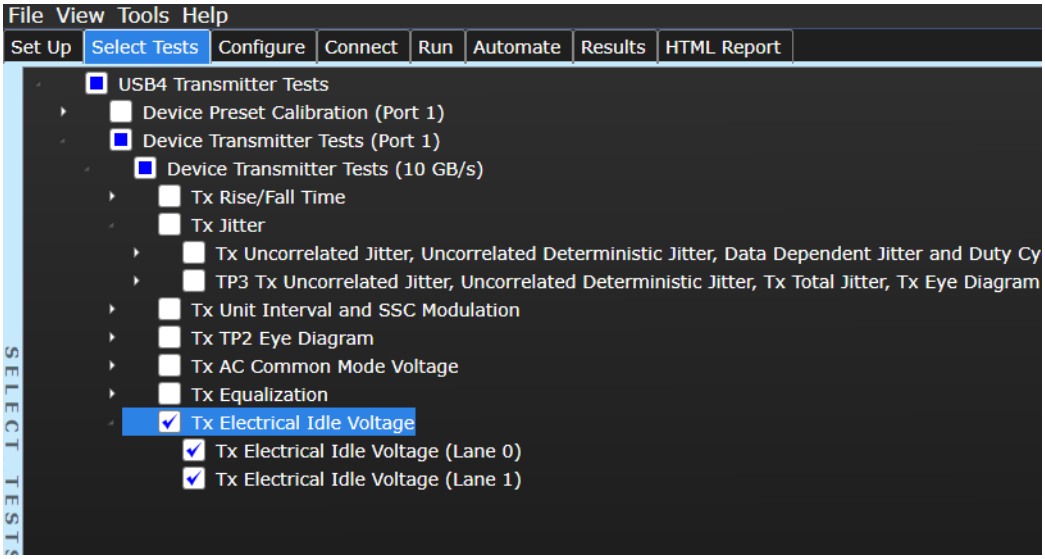


Figure 116 Selecting the Tx Electrical Idle Voltage Tests

Test Procedure

1 Configure the DUT to be in electrical idle mode.
2 Capture the waveform, and process it with the Digital Oscilloscope.
   a Sampling Rate ≥ 80 GSa/s.
   b Evaluate 10 Mpts per channel when using 80 GSa/s. For higher sampling rate, use memory depth in the same ratio to 10 Mpts.
   c No CDR, no average, and no interpolation to be used.
   d Oscilloscope must have a minimum bandwidth of 16 GHz (Gen 2) 21 GHz (Gen 3).
3 Calculate the TX Electrical Idle Voltage (V_ELEC_IDLE) using this equation:
   $V_{PEAK} = V_{TX-P} - V_{TX-N}$
4 $V_{\_ELEC\_IDLE}$ shall be extracted after applying first order low-pass filter with 3 dB point at 1.25 GHz.
5 Repeat the test for the remaining USB4 lanes.

Measurement Procedure

1 Verify the input signal.
   a Verify the input signal's amplitude.
   b Scale the vertical display of the input signal to optimum value.
2 Capture the input signal, and create the differential signal.
3 Setup the parameter of the general measurement.
   a Enable measure all edges to obtain the statistical values of the measurement.
4 Setup the following measurement:
   a Peak-to-peak voltage (V_{pp})
   b Root-mean-square voltage (V_{rms})
5 Report the Electrical Idle Output Voltage measurement results.

Expected / Observable Results

V_ELEC_IDLE > 20 mV_{p-p}, the status of test is FAIL

Test References

See

- *USB4 Specification Version 2.00 (Table 3-2)*

Tx Differential Return Loss Test

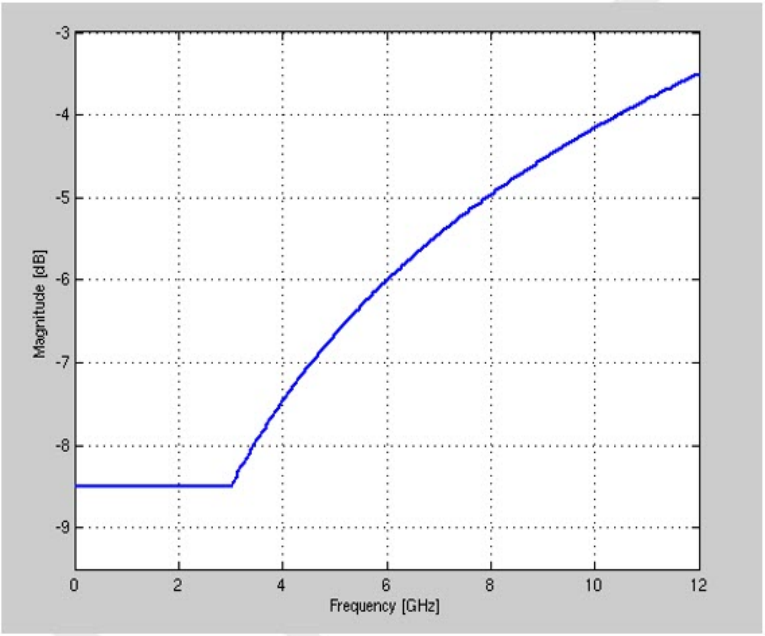
NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of this test is to confirm that the Differential Return Loss of a USB4 device is less than the maximum limit.

Test Pass Requirement

$$\mathrm{SDD11(f)} = \begin{cases} -8.5 & 0.05 < f_{GHz} \leq 3 \\ -3.5 + 8.3 \cdot \log 10\left(\frac{f_{GHz}}{12}\right) & 3 < f_{GHz} \leq 12 \end{cases}$$



Test Setup

1 For the physical connections between the DUT & the Oscilloscope, see the connection diagrams in Figure 117 and Figure 118.

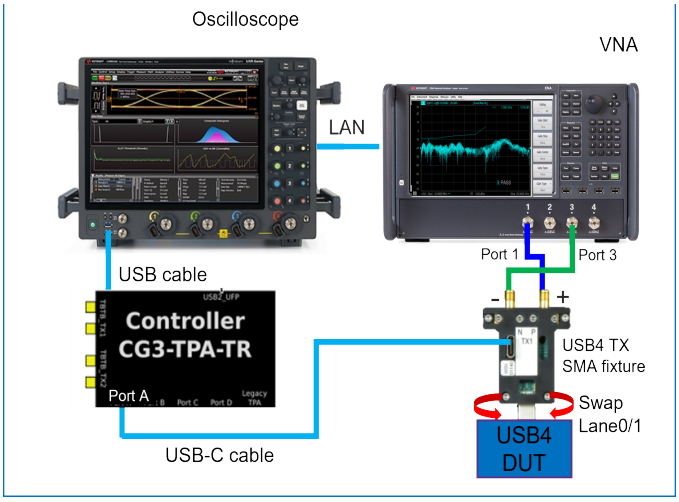


Figure 117 Tx Return loss test setup with Tx SMA test fixture

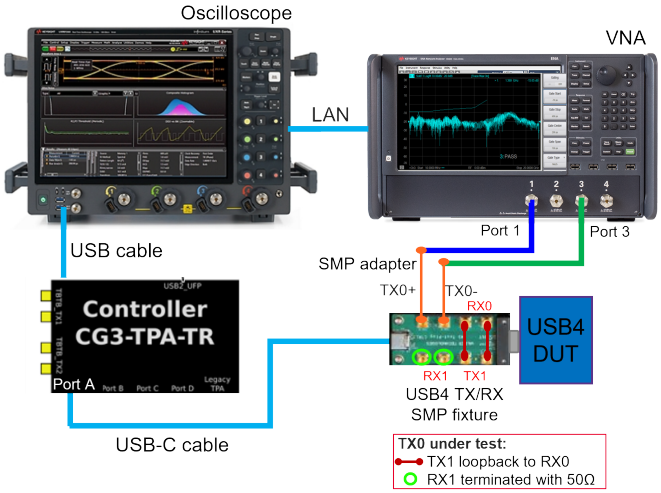
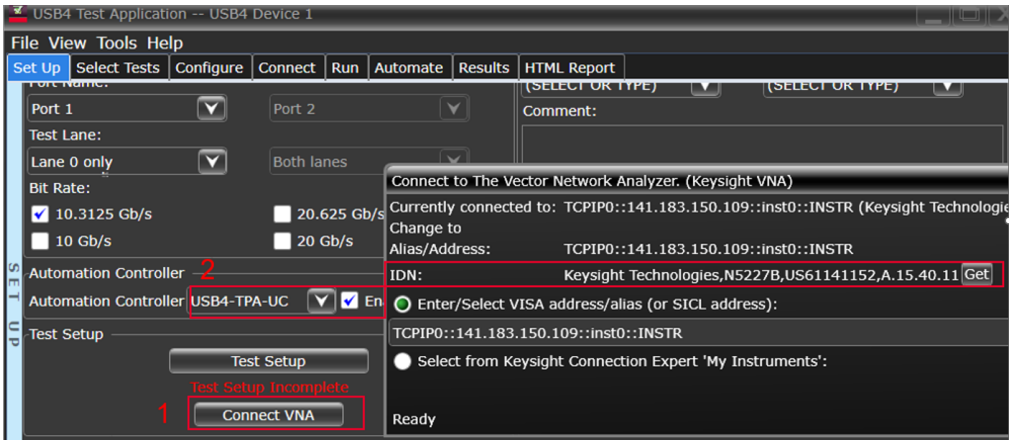


Figure 118 Return loss test setup with Tx/Rx SMP test fixture

2 In the **Set Up** tab, please connect VNA in the Tx app.

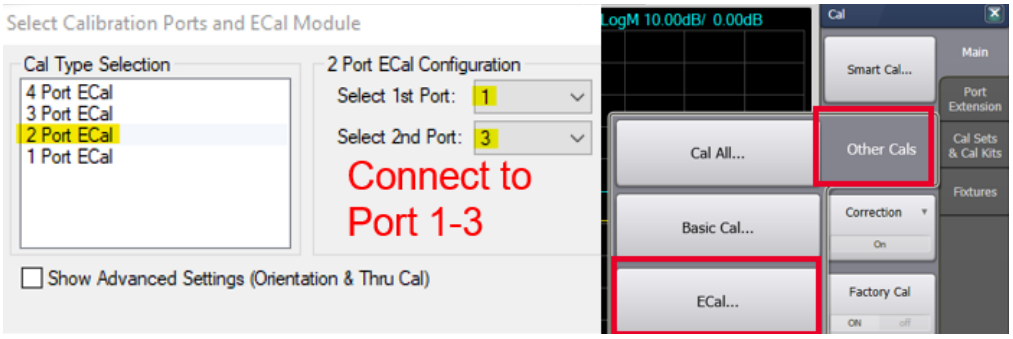


3 Prior calibration, setup Network Analyzer with following sweep settings:

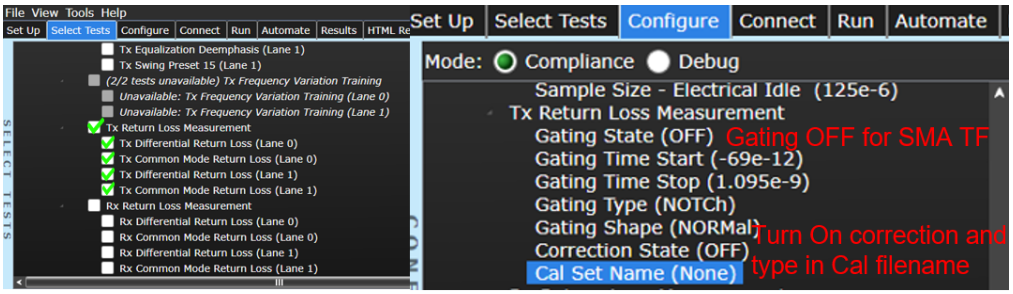
- Frequency range of 10 MHz to 12 GHz
- IF BW of 1 kHz
- At least 1600 points
- Impedance 85 ohm differential
- Define the Topology to Bal using VNA Port 1 and Port 3

NOTE Ensure that the VNA firmware revision is A.17.25.05 or higher to be compatible with the return loss test automation.

4 Run calibration on the network analyzer and test cables using a 2-port electronic kit (ECal). Save the Cal file.



5 In the **Select** test tab, select the Tx Return Loss Measurement and set the parameters in the **Configure** tab as shown in the figure below.



NOTE Please note that no gating setup is required for SMA fixture.

6 The test application sets USB4ETT **Tool Usage Mode**, commands VNA to measure Tx Return Loss in S2P, and compiles result using SigTest.

7 In the test setup, please flip the Tx fixture to swap the test lanes 0 and 1.

8 In case of SMP test fixture, Tx/Rx lane under test can be switched as shown in Figure 119.

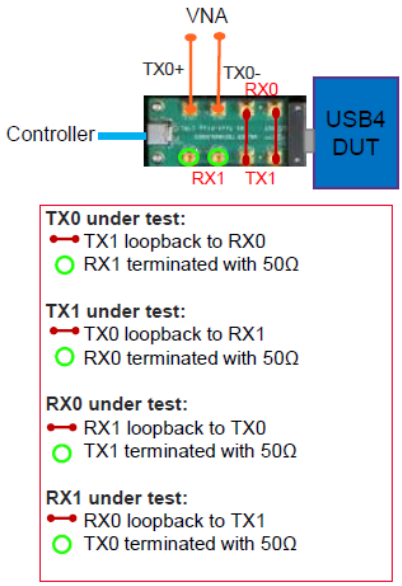


Figure 119 SMP test fixture - Tx/Rx lane switching

Test Procedure

1 Choose a supported USB4 speed to start with.
2 The test application sets USB4ETT tool to configure the DUT transmitter to output PRBS31 on all lanes with SSC turned on.
3 Connect Lane under test TX_P, TX_N to the Network Analyzer.
4 Measure the Differential R. Loss with the Network Analyzer and compile the result using SigTest.
5 If Differential Return loss violates the above requirement, then the result is Fail.
6 Repeat the test for all remaining USB4 lanes.
7 Repeat the test for all supported USB4 Gen2 and Gen3 speeds.

Expected / Observable Results

If Differential Return Loss violated the specified requirement, then Fail.

Test References

See

- *USB4 Specification Version 2.00, Table 3-2*

Tx Common Mode Return Loss Test

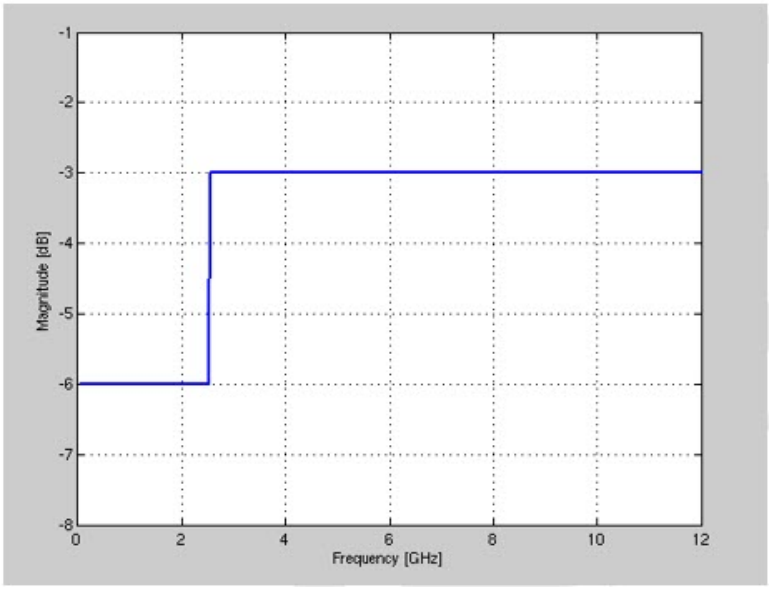
NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of this test is to confirm that the Common Mode Return Loss of a USB4 device is less than the maximum limit.

Test Pass Requirement

$$SCC11(f) = \begin{cases} -6 & 0.05 < f_{GHz} \leq 2.5 \\ -3 & 2.5 < f_{GHz} \leq 12 \end{cases}$$



Test Setup

1 For the physical connections between the DUT & the Oscilloscope, see the connection diagrams in Figure 120 and Figure 121.

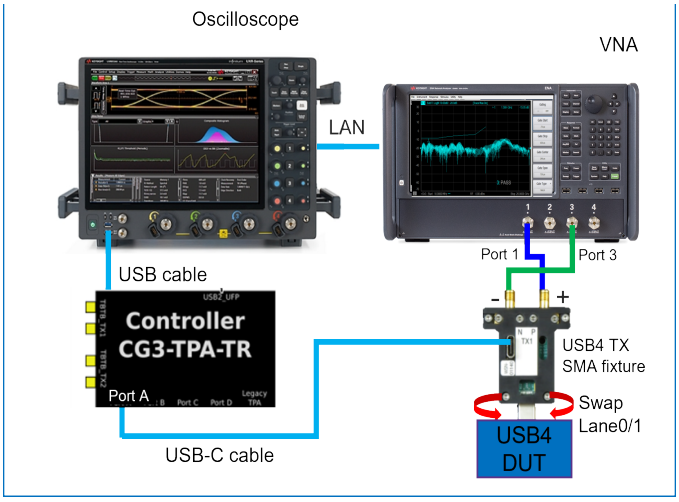


Figure 120 Tx Return loss test setup with Tx SMA test fixture

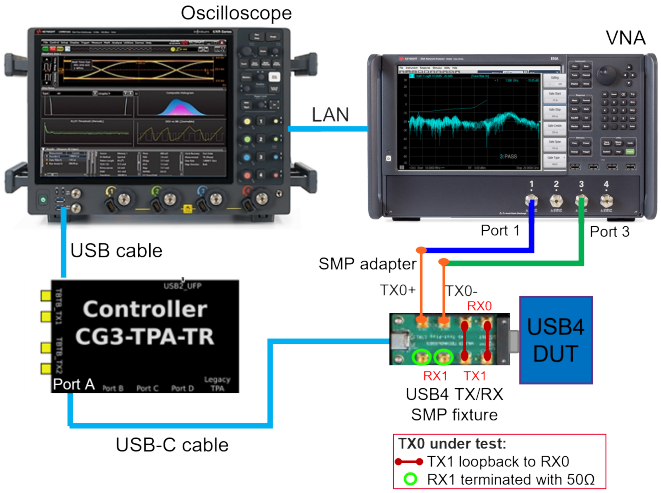
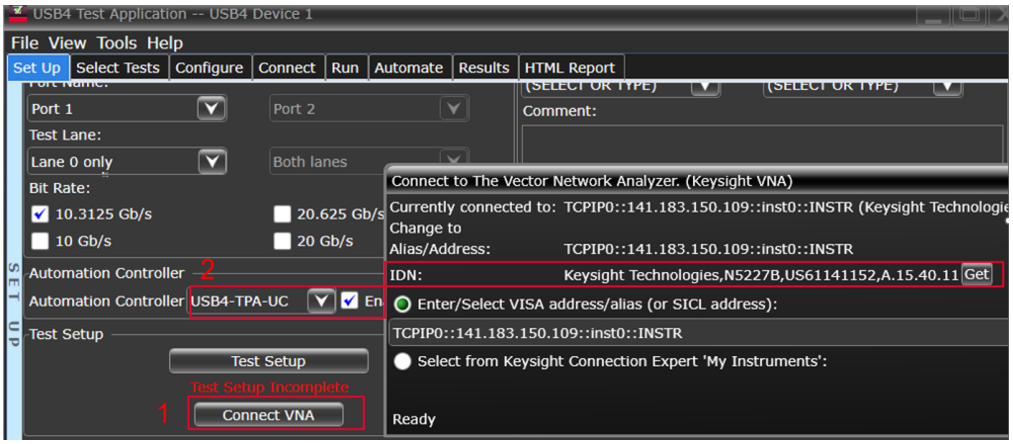


Figure 121 Return loss test setup with Tx/Rx SMP test fixture

2 In the **Set Up** tab, please connect VNA in the Tx app.

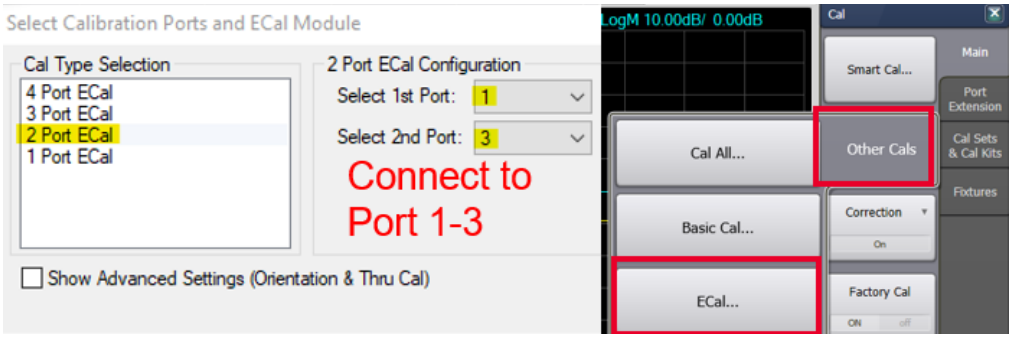


3 Prior calibration, setup Network Analyzer with following sweep settings:

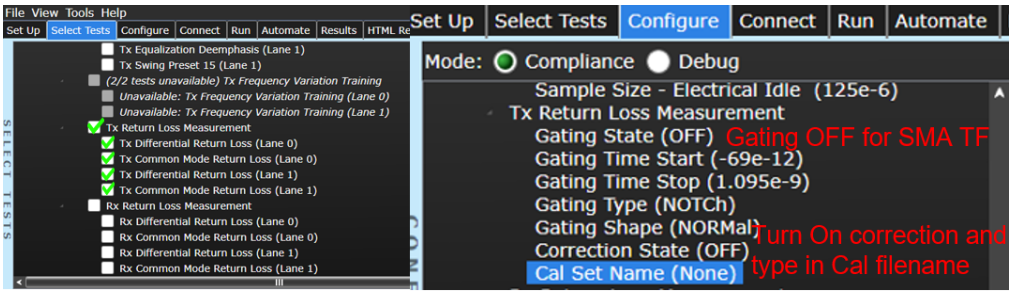
- Frequency range of 10 MHz to 12 GHz
- IF BW of 1 kHz
- At least 1600 points
- Impedance 85 ohm differential
- Define the Topology to Bal using VNA Port 1 and Port 3

NOTE Ensure that the VNA firmware revision is A.17.25.05 or higher to be compatible with the return loss test automation.

4 Run calibration on the network analyzer and test cables using a 2-port electronic kit (ECal). Save the Cal file.



5 In the **Select** test tab, select the Tx Return Loss test and set the parameters in the **Configure** tab as shown in the figure below.



NOTE Please note that no gating setup is required for SMA fixture.

6 The test application sets USB4ETT **Tool Usage Mode**, commands VNA to measure Tx Return Loss in S2P, and compiles result using SigTest.

7 In the test setup, please flip the Tx fixture to swap the test lanes 0 and 1.

8 In case of SMP test fixture, Tx/Rx lane under test can be switched as shown in Figure 122.

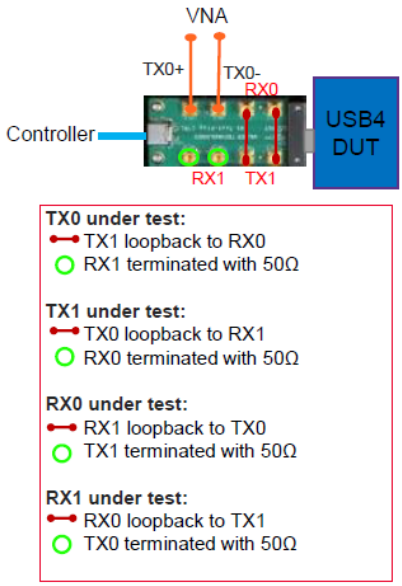


Figure 122 SMP test fixture - Tx/Rx lane switching

Test Procedure

1 Choose a supported USB4 speed to start with.
2 The test application sets USB4ETT tool to configure the DUT transmitter to output PRBS31 on all lanes with SSC turned on.
3 Connect Lane under test TX_P, TX_N to the Network Analyzer.
4 Measure the Common Mode Return Loss with the Network Analyzer and compile the result using SigTest.
5 If Common Mode Return loss violates the above requirement, then the result is Fail.
6 Repeat the test for all remaining USB4 lanes.
7 Repeat the test for all supported USB4 Gen2 and Gen3 speeds.

Expected / Observable Results

If Common Mode Return Loss violated the specified requirement, then Fail.

Test References

See

- *USB4 Specification Version 2.00, Table 3-2*

Rx Differential Return Loss Test

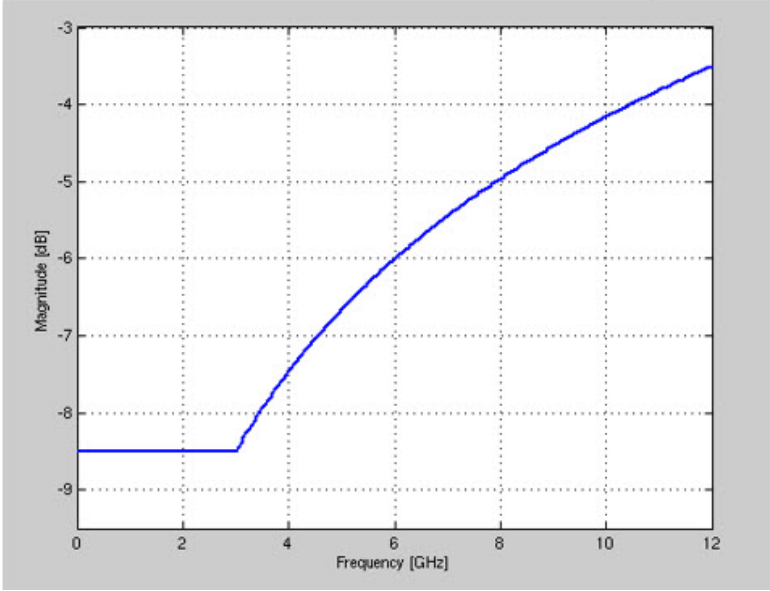
NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of this test is to confirm that the Differential Return Loss of a USB4 device is less than the maximum limit.

Test Pass Requirement

$$\mathrm{SDD22(f)} = \begin{cases} -8.5 & 0.05 < f_{GHz} \leq 3 \\ -3.5 + 8.3 \cdot \log 10\left(\frac{f_{GHz}}{12}\right) & 3 < f_{GHz} \leq 12 \end{cases}$$



Test Setup

1 For the physical connections between the DUT & the Oscilloscope, see the connection diagrams in Figure 123 and Figure 124.

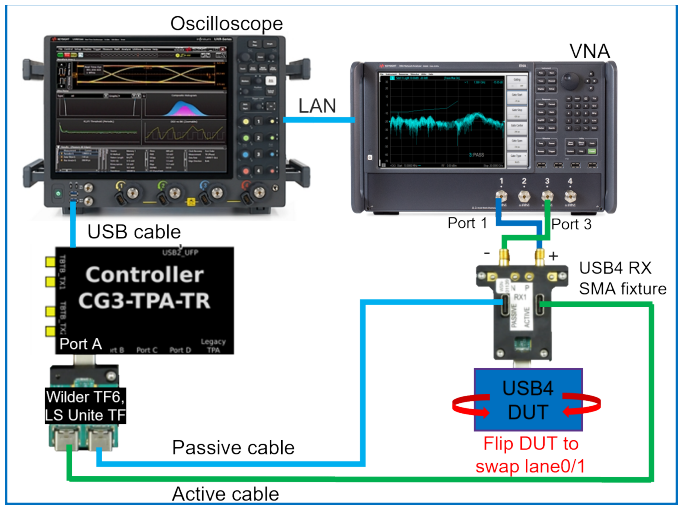


Figure 123 Tx Return loss test setup with Rx SMA test fixture

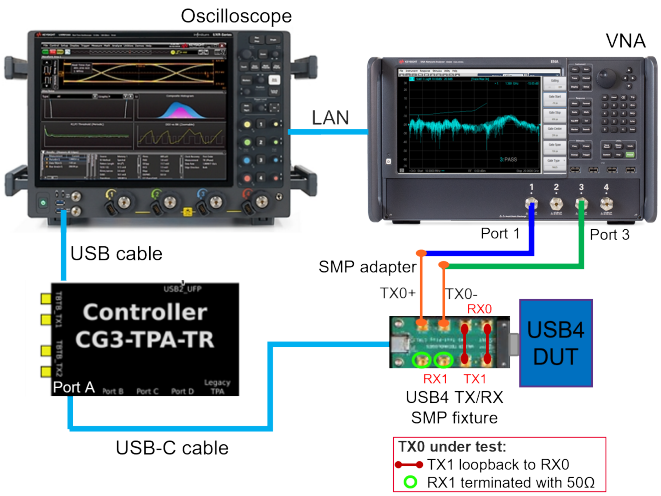
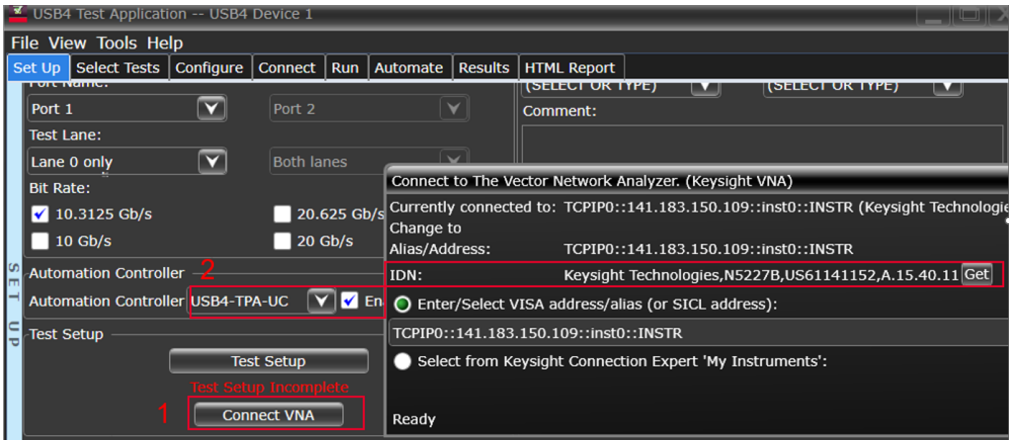


Figure 124 Return loss test setup with Tx/Rx SMP test fixture

2 In the **Set Up** tab, please connect VNA in the Tx app.

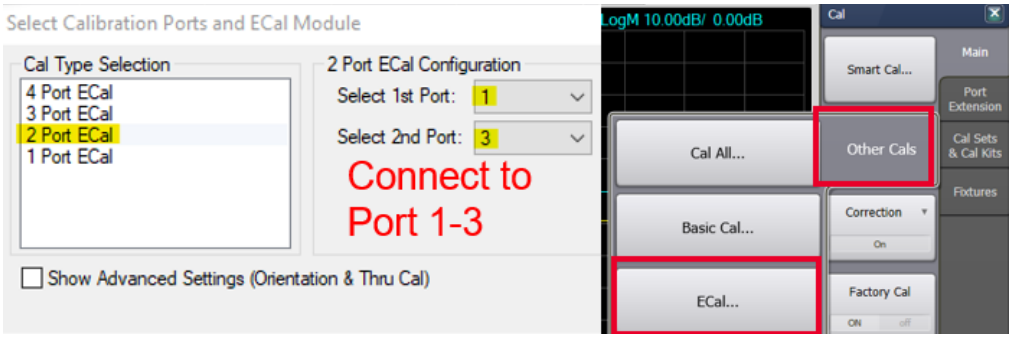


3 Prior calibration, setup Network Analyzer with following sweep settings:

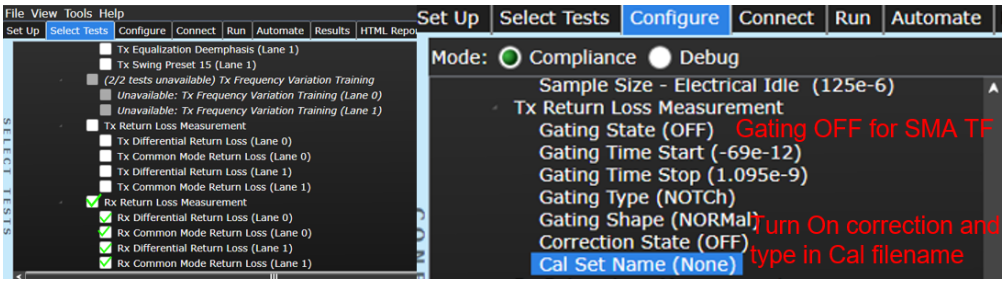
- Frequency range of 10 MHz to 12 GHz
- IF BW of 1 kHz
- At least 1600 points
- Impedance 85 ohm differential
- Define the Topology to Bal using VNA Port 1 and Port 3

NOTE Ensure that the VNA firmware revision is A.17.25.05 or higher to be compatible with the return loss test automation.

4 Run calibration on the network analyzer and test cables using a 2-port electronic kit (ECal). Save the Cal file.



5 In the **Select** test tab, select the Tx Return Loss test and set the parameters in the **Configure** tab as shown in the figure below.



NOTE Please note that no gating setup is required for SMA fixture.

6 The test application sets USB4ETT **Tool Usage Mode**, commands VNA to measure Tx Return Loss in S2P, and compiles result using SigTest.

7 In the test setup, please flip the Rx fixture to swap the test lanes 0 and 1.

8 In case of SMP test fixture, Tx/Rx lane under test can be switched as shown in Figure 125.

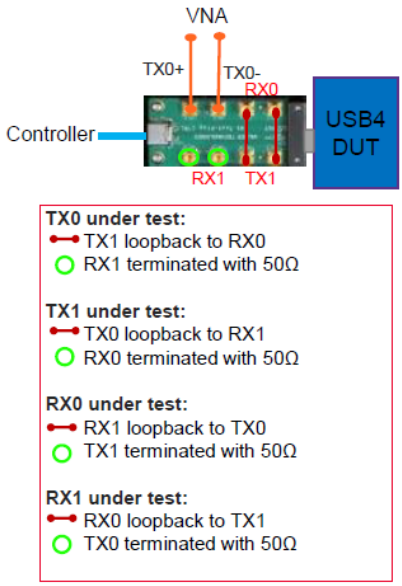


Figure 125 SMP test fixture - Tx/Rx lane switching

Test Procedure

1 Choose a supported USB4 speed to start with.
2 The test application sets USB4ETT tool to configure the DUT transmitter to output PRBS31 on all lanes with SSC turned on.
3 Connect a USB Type-C Passive cable from the Passive receptacle connector over the test fixture to the Low speed united coupon Passive receptacle connector that is connected to the USB4 Micro-controller PA.
4 Connect a USB Type-C Active cable from the Active receptacle connector over the test fixture to the Low speed united coupon Active receptacle connector that is connected to the USB4 Micro-controller PA.
5 Connect Lane under test RX_P, RX_N to the Network Analyzer.
6 Measure the Differential R. Loss with the Network Analyzer and compile the result using SigTest.
7 If Differential Return loss violates the above requirement, then the result is Fail.
8 Repeat the test for all remaining USB4 lanes.
9 Repeat the test for all supported USB4 Gen2 and Gen3 speeds.

Expected / Observable Results

If Differential Return Loss violated the specified requirement, then Fail.

Test References

See

- *USB4 Specification Version 2.00, Table 3-9*

Rx Common Mode Return Loss Test

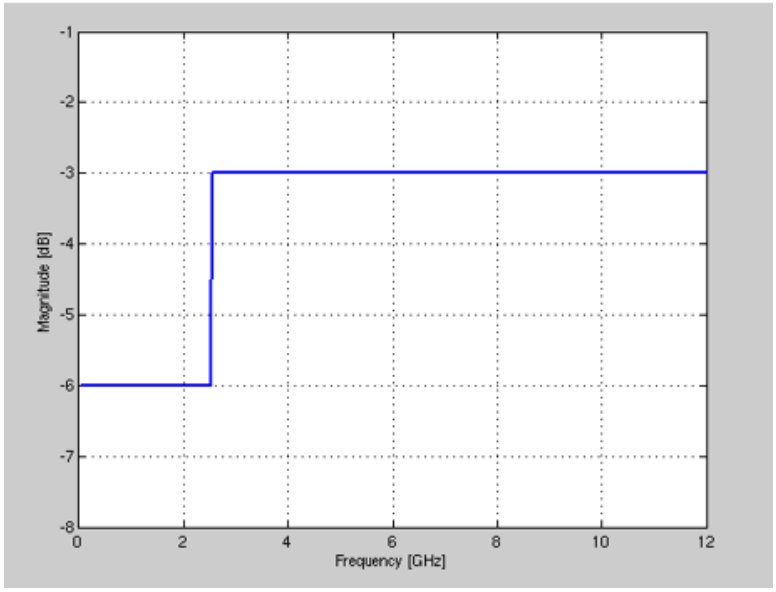
NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of this test is to confirm that the Common Mode Return Loss of a USB4 device is less than the maximum limit.

Test Pass Requirement

$$SCC22(f) = \begin{cases} -6 & 0.05 < f_{GHz} \leq 2.5 \\ -3 & 2.5 < f_{GHz} \leq 12 \end{cases}$$



Test Setup

1 For the physical connections between the DUT & the Oscilloscope, see the connection diagrams in Figure 126 and Figure 127.

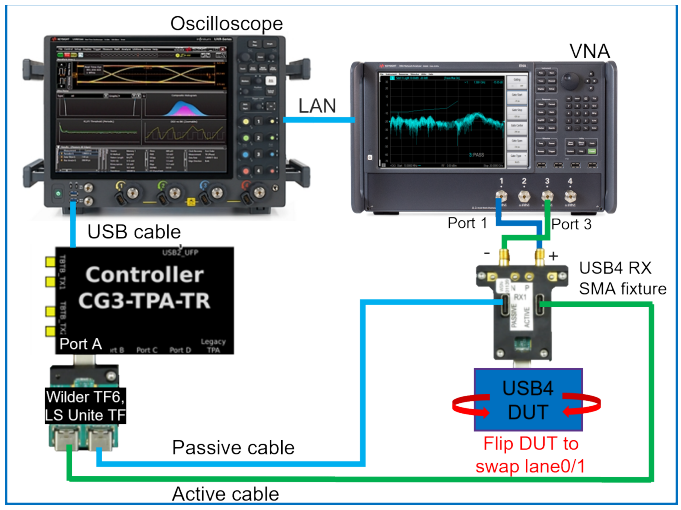


Figure 126 Tx Return loss test setup with Rx SMA test fixture

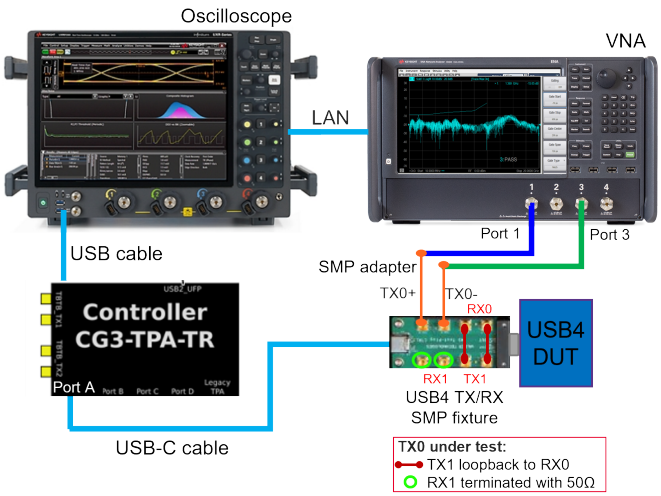
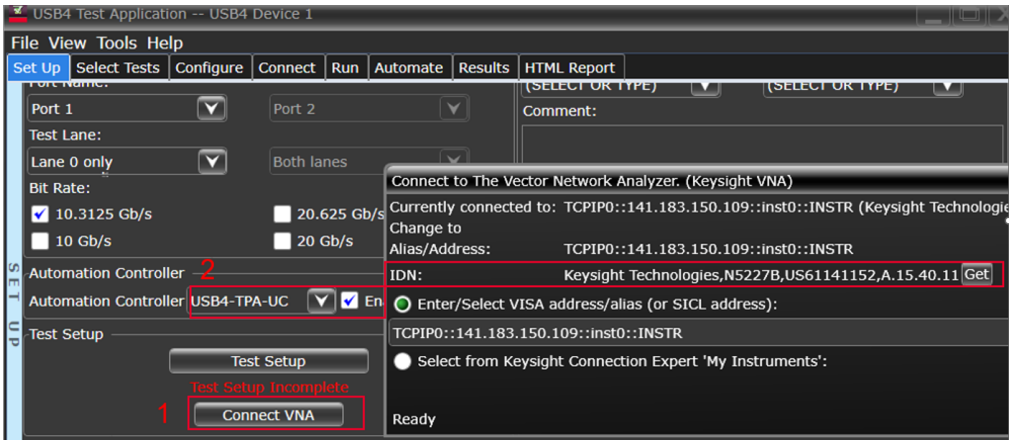


Figure 127 Return loss test setup with Tx/Rx SMP test fixture

2 In the **Set Up** tab, please connect VNA in the Tx app.

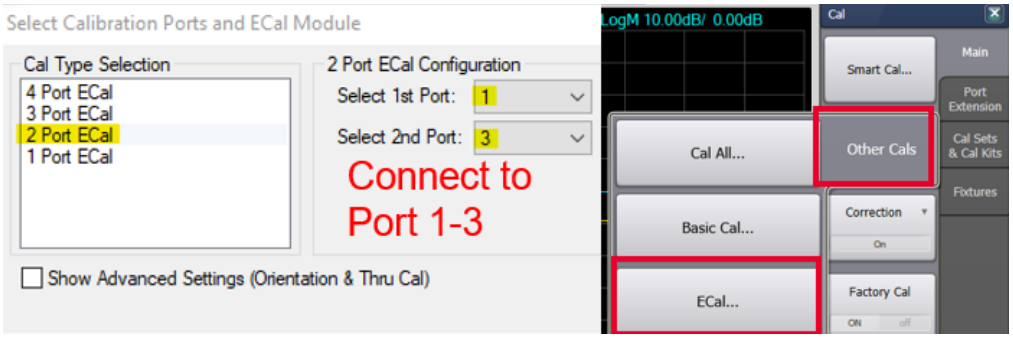


3 Prior calibration, setup Network Analyzer with following sweep settings:

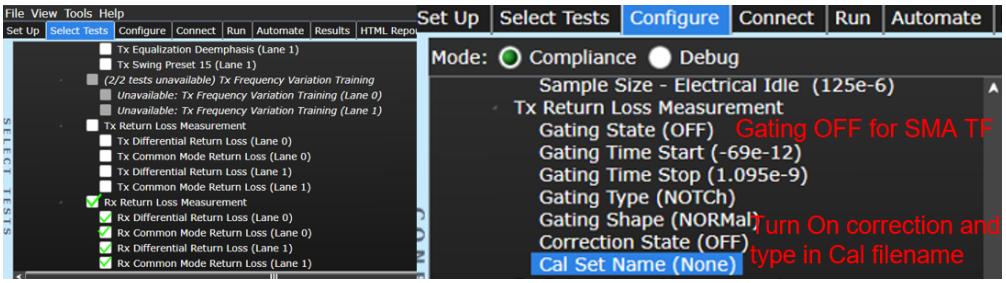
- Frequency range of 10 MHz to 12 GHz
- IF BW of 1 kHz
- At least 1600 points
- Impedance 85 ohm differential
- Define the Topology to Bal using VNA Port 1 and Port 3

NOTE Ensure that the VNA firmware revision is A.17.25.05 or higher to be compatible with the return loss test automation.

4 Run calibration on the network analyzer and test cables using a 2-port electronic kit (ECal). Save the Cal file.



5 In the **Select** test tab, select the Tx Return Loss test and set the parameters in the **Configure** tab as shown in the figure below.



NOTE Please note that no gating setup is required for SMA fixture.

6 The test application sets USB4ETT **Tool Usage Mode,** commands VNA to measure Tx Return Loss in S2P, and compiles result using SigTest.

7 In the test setup, please flip the Rx fixture to swap the test lanes 0 and 1.

8 In case of SMP test fixture, Tx/Rx lane under test can be switched as shown in Figure 128.

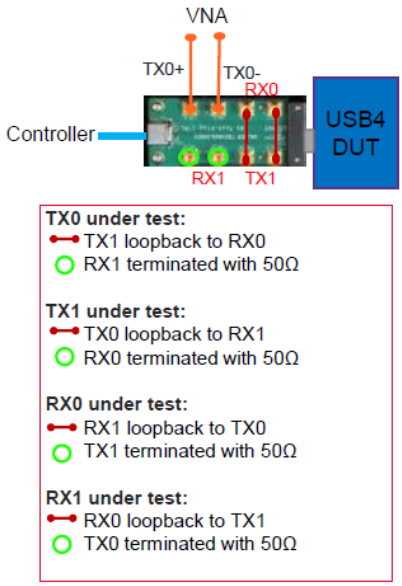


Figure 128 SMP test fixture - Tx/Rx lane switching

Test Procedure

1 Choose a supported USB4 speed to start with.
2 The test application sets USB4ETT tool to configure the DUT transmitter to output PRBS31 on all lanes with SSC turned on.
3 Connect a USB Type-C Passive cable from the Passive receptacle connector over the test fixture to the Low speed united coupon Passive receptacle connector that is connected to the USB4 Micro-controller.
4 Connect a USB Type-C Active cable from the Active receptacle connector over the test fixture to the Low speed united coupon Active receptacle connector that is connected to the USB4 Micro-controller.
5 Connect Lane under test RX_P, RX_N to the Network Analyzer.
6 Measure the Common Mode Return Loss with the Network Analyzer and compile the result using SigTest.
7 If Common Mode Return loss violates the above requirement, then the result is Fail.
8 Repeat the test for all remaining USB4 lanes.
9 Repeat the test for all supported USB4 Gen2 and Gen3 speeds.

Expected / Observable Results

If Common Mode Return Loss violated the specified requirement, then Fail.

Test References

See

USB4 Specification Version 2.00, Table 3-9

7 Transmitter Tests for 20.625 GB/s Systems

Tx Preset Calibration / 262
SBTX High Voltage / 266
SBTX Low Voltage / 268
SBTX Rise/Fall Time / 270
SBTX UI Duration / 273
SBRX High Voltage Detection / 276
SBRX Low Voltage Detection / 278
Tx Rise/Fall Time / 279
Tx Uncorrelated Jitter / 281
Tx Uncorrelated Deterministic Jitter / 283
Tx Data Dependent Jitter / 285
Tx Duty Cycle Distortion / 287
Tx Low Frequency Uncorrelated Deterministic Jitter / 289
Tx Total Jitter / 291
Tx Uncorrelated Jitter TP3 / 293
Tx Uncorrelated Deterministic Jitter TP3 / 295
Tx Total Jitter TP3 / 297
Tx Eye Diagram TP3 / 300
Tx Minimum Unit Interval Min/Max / 303
Tx SSC Down Spread Rate / 305
Tx SSC Down Spread Range / 307
Tx SSC Slew Rate / 309
Tx SSC Phase Deviation / 311
Tx Eye Diagram / 313
Tx AC Common Mode Voltage / 316
Tx Equalization Tests / 318
Tx Electrical Idle Voltage Test / 323
Tx Differential Return Loss Test / 325
Tx Common Mode Return Loss Test / 330
Rx Differential Return Loss Test / 335
Rx Common Mode Return Loss Test / 340

This section provides the Methods of Implementation (MOIs) to run electrical tests on a USB DUT operating at a bit rate of 20.625 GB/s using an Keysight Infiniium Oscilloscope and other accessories, along with the Keysight D9040USBC USB4 Compliance Test Application.

NOTE All USB4 devices that support a bit rate of 20.625 Gb/s are classified as Gen3 devices.

Tx Preset Calibration

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Preset Calibration Test is to find the optimized preset for the platform.

NOTE Prior to running the compliance tests, the Host / Device must go through Preset Calibration.

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 130 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Preset Calibration* are checked.

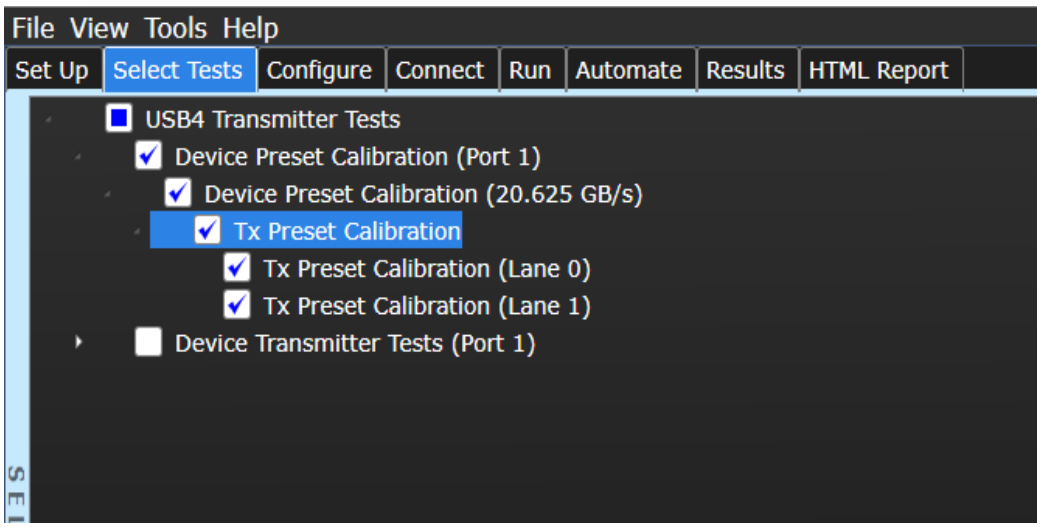


Figure 129 Selecting the Tx Preset Calibration tests

NOTE

By default, the test group for **Preset Calibration** for each selected bit-rate is hidden in the **Select Tests** tab when **Predefined Optimum Preset Number** is selected for the respective bit-rates. To view and select the **Preset Calibration** tests in the **Select Tests** tab, select the **Run Preset Calibration** option in the **Test Setup** window of the **Set Up** tab.

NOTE

In the **Measurement Server** mode or **Multi** instance mode, it is recommended to run the **Tx Preset Calibration** tests first to get the optimized preset value. Then use this value to run the remaining transmitter tests.

Detailed Process:

In the **Measurement Server** mode or **Multi** instance mode, after running the **Preset Calibration** test, please see the HTML Report and note down the optimized preset value. Then, please navigate to **Set Up** tab > **Test Setup** button > **Test Setup** dialog box. Select the check box “Predefined Optimum Preset Number”, use the already noted optimized preset number, and manually **Select the Optimum Preset Number for Each Bit Rate**. Now, please run the rest of the transmitter tests.

USB4 Microcontroller and Test Adapter USB Test Set-up

The figure, below, shows a simplified set-up example of a USB4 Microcontroller and a US4B Test Adapter used to test a typical USB DUT.

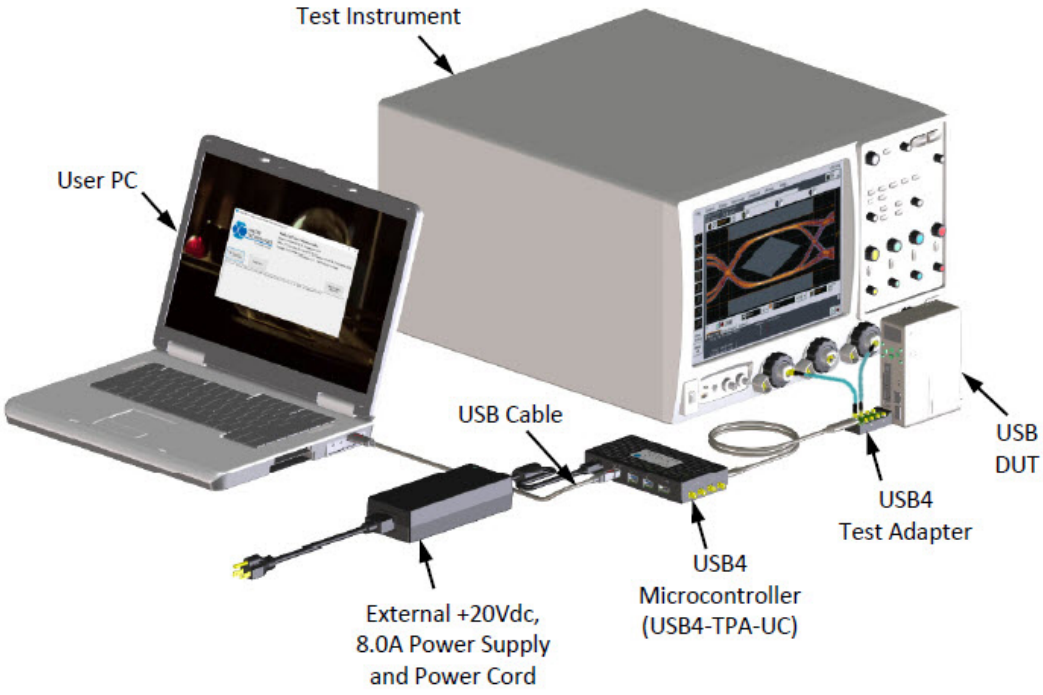


Figure 130 Transmitter TP2/TP3 Test Setup

Test Procedure

1 Connect the DUT to the Oscilloscope as shown in the Figure 130.
2 Choose a USB4 speed to start with.
3 Configure the DUT transmitter to output PRBS15, preset 0 on all lanes with SSC enabled.
4 The cables from the plug test fixture to the scope shall be de-embedded.
5 Perform measurements with:
   a Reference CDR modeled by a 2^{nd} order PLL response which drives High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used.
   b Oscilloscope with a minimum bandwidth of 21 GHz.
6 Capture the waveform and process it with the digital oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Evaluate 40 Mpts per channel when using 80 GSa/s. For higher sample rate use memory depth in the same ration to 40 Mpts.
   c Pattern length - Periodic
   d Jitter separation method shall be suitable for cross talk on signal
   e Adjust vertical scale to fit signal into scope screen.
   f Referenced to 1E-13 statistics.
7 Capture DDJ results for lane 0.
8 Repeat the test for all remaining USB4 transmit presets (till preset 15 as shown in Table 5).
9 Repeat the test for the remaining USB4 lanes.
10 For each lane, choose the preset that provides minimum DDJ.
11 Repeat the above procedure for all supported USB4 speeds.

Expected / Observable Results

For each lane, the preset that provides the minimum DDJ is the optimized preset for the platform.

Test References

See

- USB4 Specification Version 2.00 (Table 3-5)

SBTX High Voltage

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of this test is to confirm that the SBTX High Voltage Measurement of a USB4 device is within the specification limits.

Test Pass Requirement

2.40 V ≤ SBTX High Voltage Measurement ≤ 3.52 V

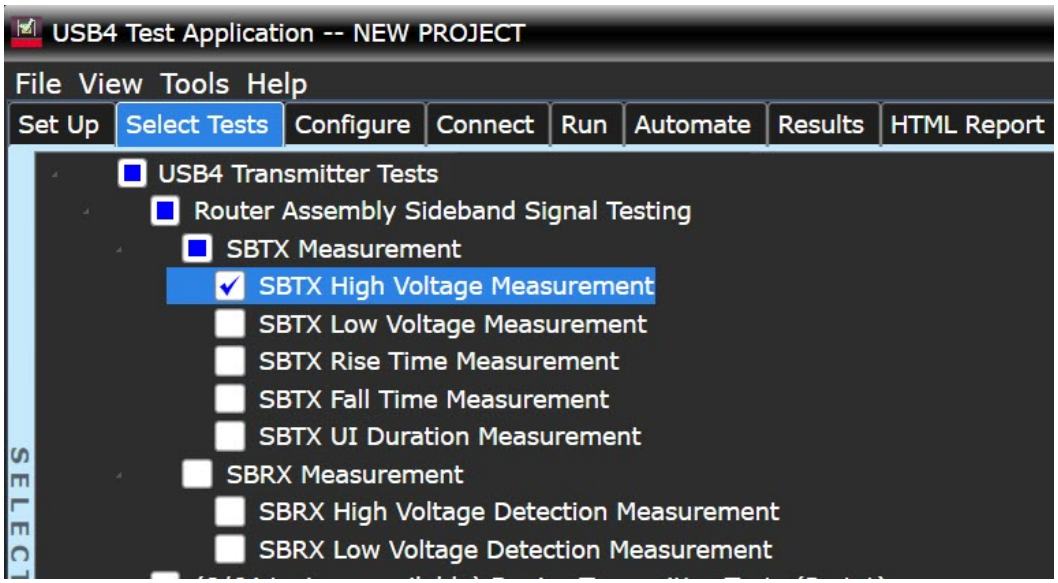
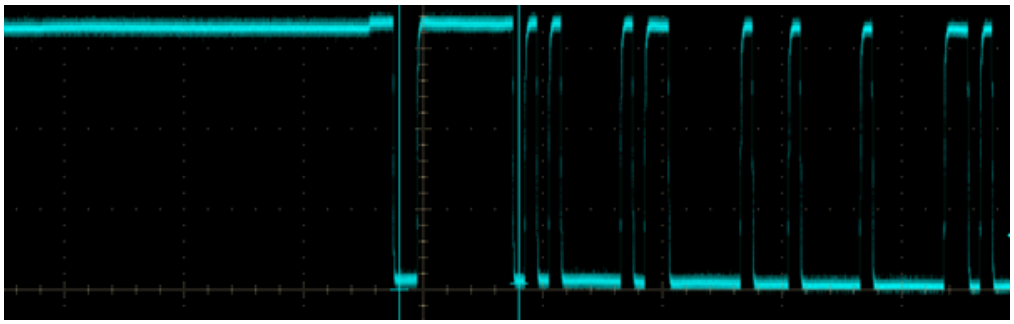


Figure 131 Selecting the SBTX High Voltage Measurement test

Test Procedure

1 Connect a voltage meter/DMMfluke to SBU1 header in the USB4 Test Fixture.
2 Power up the DUT.
3 Measure the voltage.
4 If $SBTX_{VOH}$ < 2.4 V or > 3.52 V then Fail.
5 Connect a scope with high impedance probe to the SBU1 header in the USB4 Test Fixture.
6 In the scope use a trigger based on pulse width, negative polarity, trigger when the pulse width <10 µs and threshold of 600 mV.
7 Horizontal scale = 10 µs per square, vertical scale = 1 V per square.
8 Power up the DUT.

9 Over the Infiniium Oscilloscope the trigger shall capture the transaction pattern.



10 Measure the high/low value of the "1" amplitude for a bit inside the transaction. Over/undershoot shall be ignored.

11 If $SBTX_{VOH}$ < 2.4 V or > 3.52 V then Fail.

Expected / Observable Results

If $SBTX_{VOH}$ < 2.4 V or > 3.52 V then Fail.

Test References

See

- *USB4 Specification Version 2.00 (Table 3-32)*

SBTX Low Voltage

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of this test is to confirm that the SBTX Low Voltage Measurement of a USB4 device is within the specification limits.

Test Pass Requirement

2.40 V ≤ SBTX Low Voltage Measurement ≤ 3.52 V

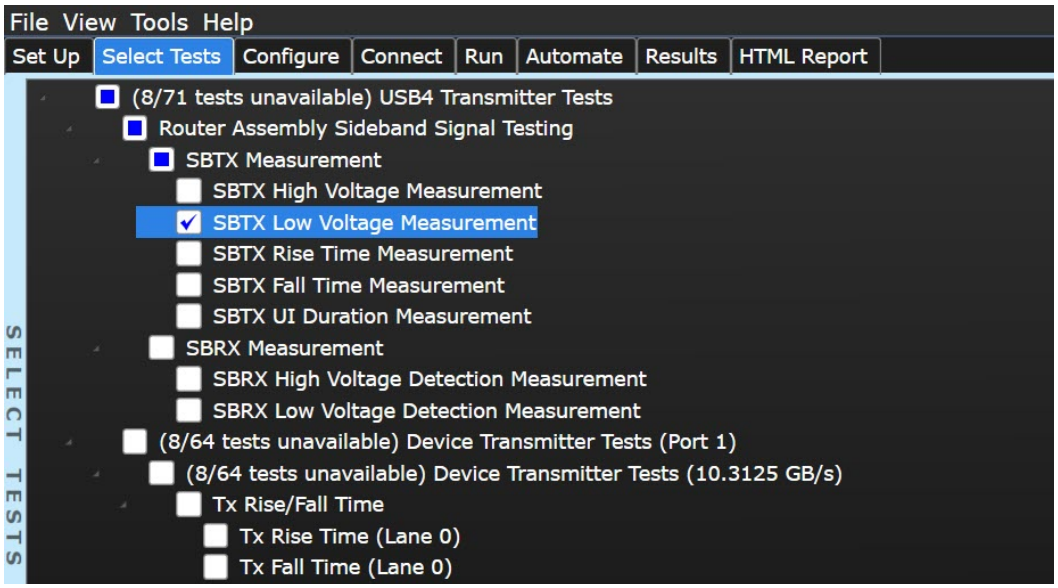


Figure 132 Selecting the SBTX Low Voltage Measurement test

Test Procedure

1. Connect a voltage meter/DMMfluke to SBU1 header in the USB4 Test Fixture.
2. DUT shall be in power down state.
3. Measure the voltage.
4. If $SBTX_{VOL}$ < -0.05 V or > 0.4 V then Fail.
5. Connect a scope with high impedance probe to the SBU1 header in the USB4 Test Fixture.
6. In the scope use a trigger based on pulse width, negative polarity, trigger when the pulse width <10 µs and threshold of 600 mV.
7. Horizontal scale = 10 µs per square, vertical scale = 1 V per square.
8. Connect link partner to the DUT.
9. Over the Infiniium Oscilloscope the trigger shall capture the transaction pattern.

10 Measure the high/low value of the "0" amplitude for a bit inside the transaction. Over/undershoot shall be ignored.

11 If $SBTX_{VOL}$ < -0.05 V or > 0.4 V then Fail.

Expected / Observable Results

If $SBTX_{VOL}$ < -0.05 V or > 0.4 V then Fail.

Test References

See

- *USB4 Specification Version 2.00 (Table 3-32)*

SBTX Rise/Fall Time

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of this test is to confirm that the SBTX Rise/Fall Time Measurement of a USB4 device is within the specification limits.

Test Pass Requirement

$3.5\ ns \leq SBX_{TRTF} \leq 65\ ns$.

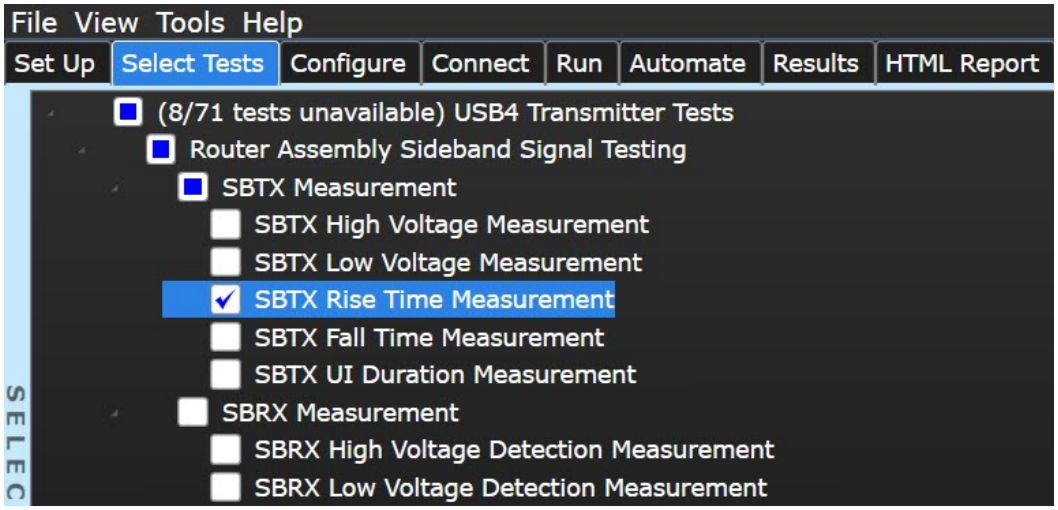


Figure 133 Selecting the SBTX Rise Time Measurement test

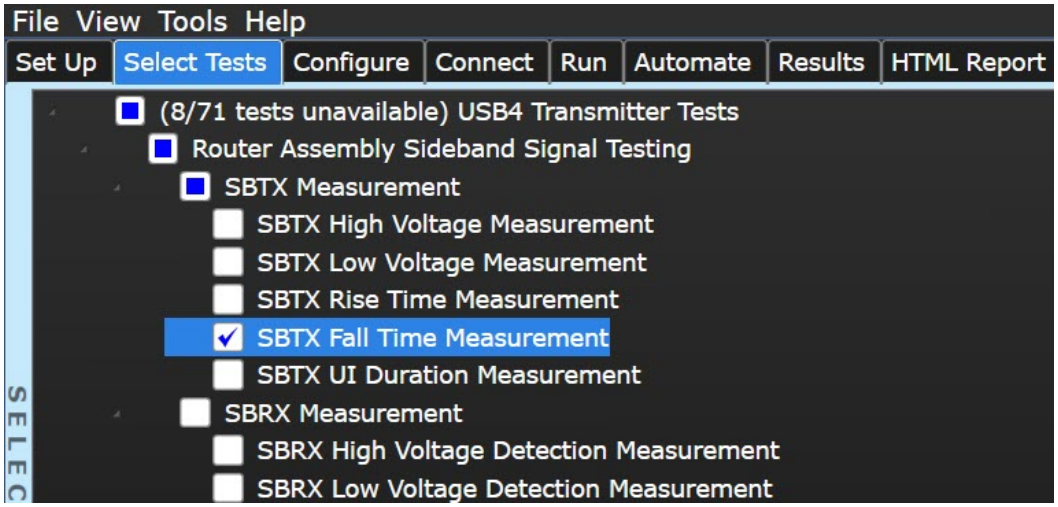
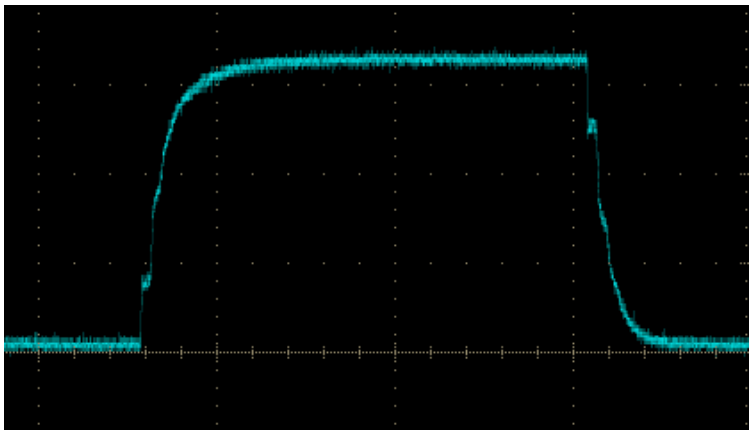


Figure 134 Selecting the SBTX Fall Time Measurement test

Test Procedure

1 Connect the DUT via USB4 Test Fixture with USB4 u-controller in order to establish link.
2 The measurement shall be in transaction only and not from power down to up (or the opposite).
3 Connect a scope with high impedance probe to the SBU1 header for SBTX test in the USB4 Test Fixture.
4 In the scope use a trigger based on pulse width, negative polarity, trigger when the pulse width <10 µs and threshold of 600 mV.
5 Horizontal scale = 10 µs per square, vertical scale = 1 V per square.
6 Power up the DUT.
7 Over the Infiniium Oscilloscope the trigger shall capture the transaction pattern.
8 Zoom in one bit from inside the transaction pattern. Not the 1st or the last bit.



9 Measure the rise and fall time (10%-90%) for SBTX.
10 If 65 ns < STX_{TRTF} < 3.5 ns then Fail.

Expected / Observable Results

If 65 ns < STX_{TRTF} < 3.5 ns then Fail.

Test References

See

- *USB4 Specification Version 2.00 (Table 3-32)*

SBTX UI Duration

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of this test is to confirm that the SBTX UI Duration Measurement of a USB4 device is within the specification limits.

Test Pass Requirement

970 ns ≤ SBX_{UI} ≤ 1030 ns.

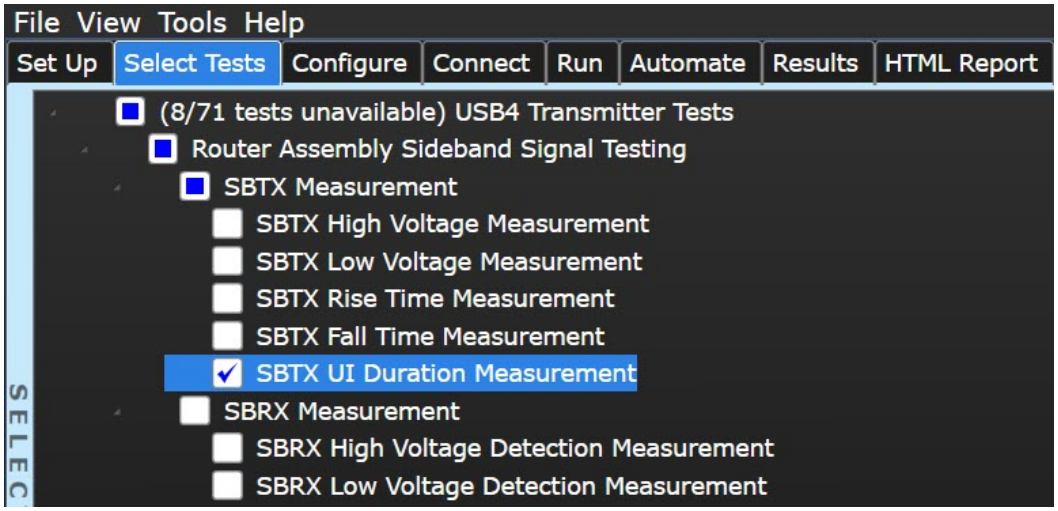
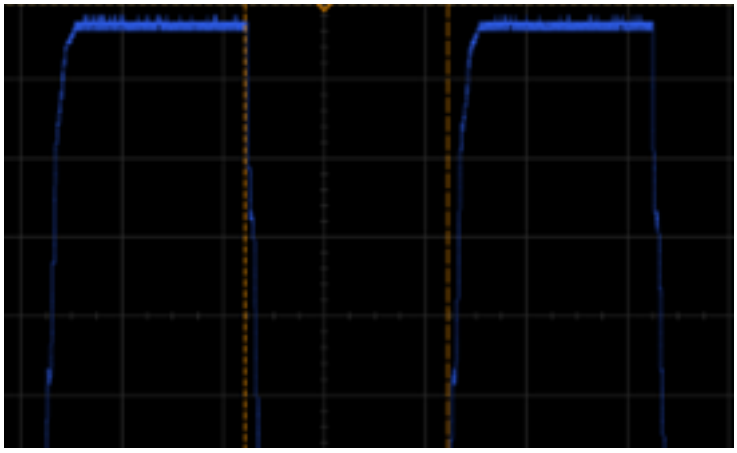


Figure 135 Selecting the SBTX UI Duration Measurement test

Test Procedure

1 Connect the DUT via USB4 Test Fixture with USB4 u-controller in order to establish link.
2 The measurement shall be in transaction only, over the transaction pattern.
3 Connect a scope with high impedance probe to the SBU1 header for SBTX test in the USB4 Test Fixture.
4 In the scope use a trigger based on pulse width, negative polarity, trigger when the pulse width <10 µs and threshold of 600 mV.
5 Horizontal scale = 10 µs per square, vertical scale = 1 V per square.
6 Power up the DUT.
7 Over the Infiniium Oscilloscope the trigger shall capture the transaction pattern.
8 Zoom in "10" bits from the transaction pattern.



9 Measure the duration from falling edge of the "1" to the rising edge of "0", named SBX_UI.
10 If 970 ns < $SBTX_{UI}$ < 1030 ns then Fail.

Expected / Observable Results

If 970 ns < $SBTX_{UI}$ < 1030 ns then Fail.

Test References

See

- *USB4 Specification Version 2.00 (Table 3-32)*

SBRX High Voltage Detection

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of this test is to confirm that the SBRX High Voltage Detection Measurement of a USB4 device is within the specification limits.

Test Pass Requirement

$2.0\ V \leq SBRX_{VIH} \leq 3.77\ V$

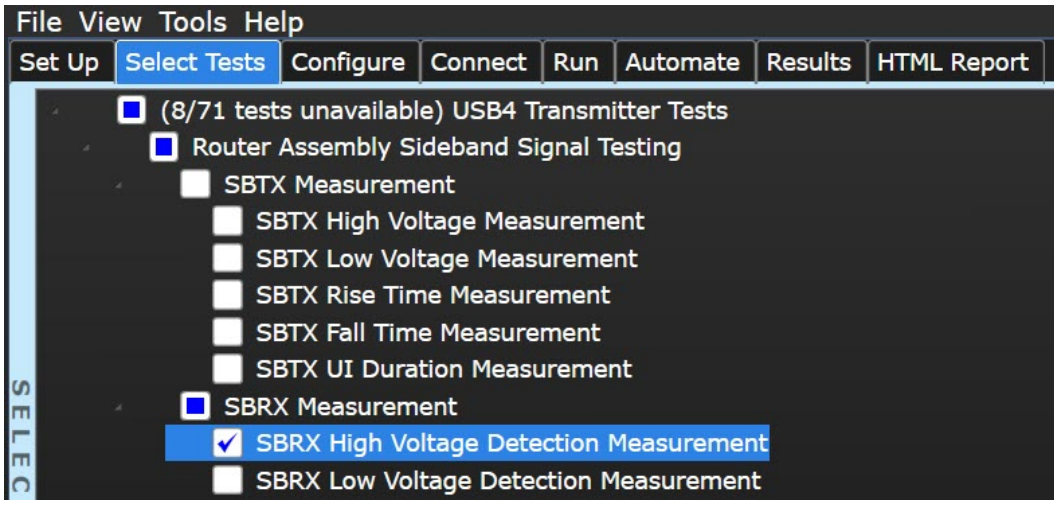
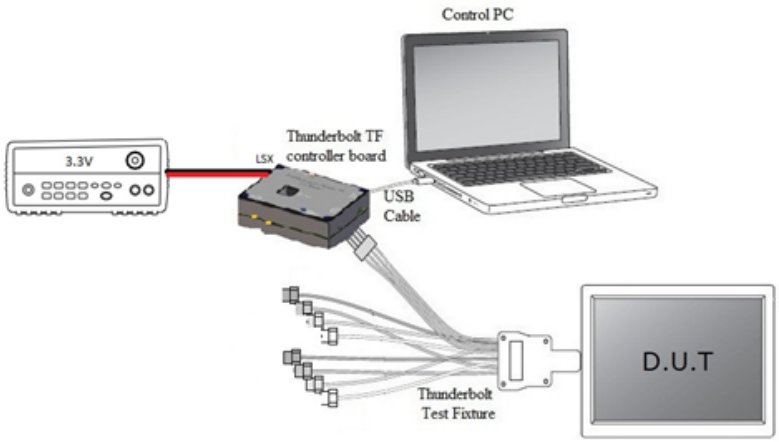


Figure 136 Selecting the SBRX High Voltage Measurement test

Test Procedure

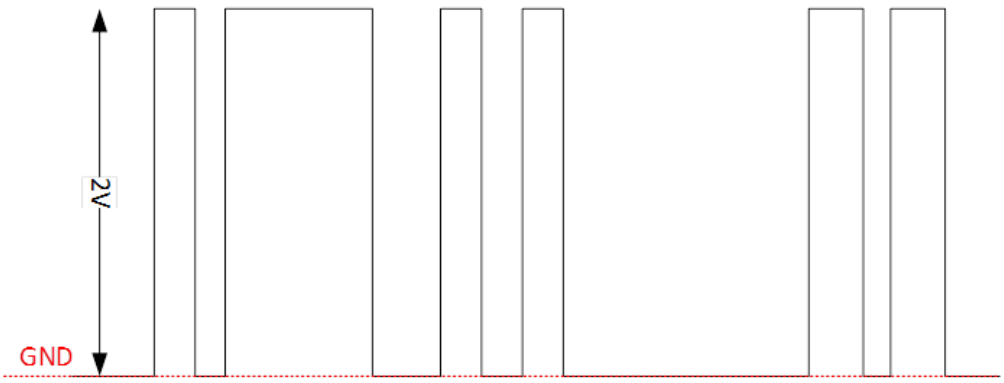
1 Connect the DUT via USB4 LSXX Test Fixture with USB4 u-controller and set '1' bit amplitude to 3.3 V and '0' bit amplitude to 0 V in order to establish link.



2 Set the 3.3 V power supply to 3.77 V.

3 Establish there is a link.

4 Reduce the external power supply to 2.0 V.



5 If link is lost, then Fail.

Expected / Observable Results

2.0 V ≤ $SBRX_{VIH}$ ≤ 3.77 V

Test References

See

- *USB4 Specification Version 2.00 (Table 3-32)*

SBRX Low Voltage Detection

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of this test is to confirm that the SBRX Low Voltage Detection Measurement of a USB4 device is within the specification limits.

Test Pass Requirement

$-0.3\ V \leq SBRX_{VIL} \leq 0.65\ V$

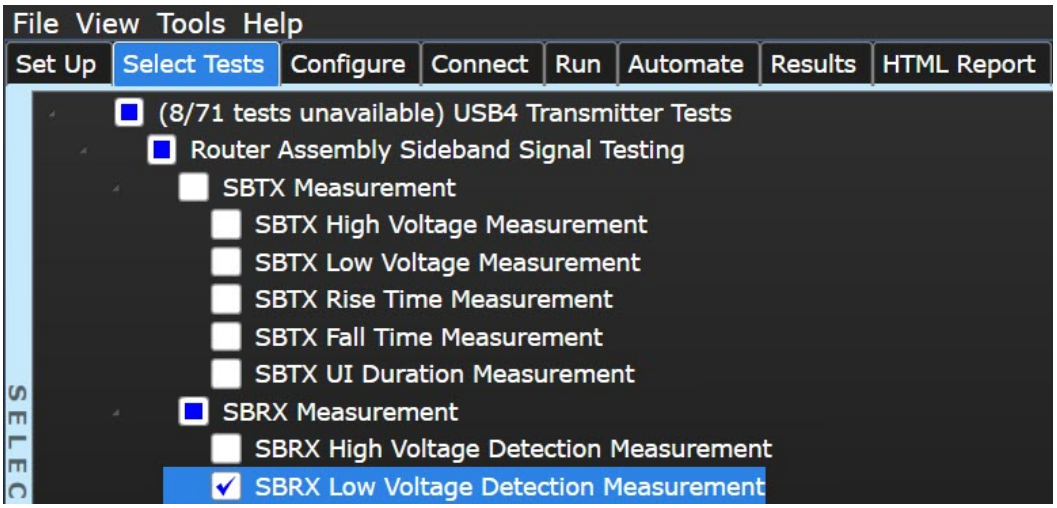


Figure 137 Selecting the SBRX Low Voltage Measurement test

Test Procedure

1. Connect the DUT via USB4 Test Fixture with USB4 u-controller with external 3.3 V power supply connected to the SBX input in order to establish link.
2. Set the 3.3 V power supply to 3.3 V.
3. Establish there is a link.
4. Reduce the external power supply to 0.65 V.
5. If link is established, then Fail.

Expected / Observable Results

$-0.3\ V \leq SBRX_{VIL} \leq 0.65\ V$

Test References

See

- *USB4 Specification Version 2.00 (Table 3-32)*

Tx Rise/Fall Time

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Rise/Fall Time Test is to confirm that the rise times and fall times on the USB differential signals are within the limits of the specification.

Test Pass Requirement

Rise Time and Fall Time $\geq$ 10.00 ps (Refer to Table 3 on page 74).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 130 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the tests under the test group *Tx Rise/Fall Time* are checked.

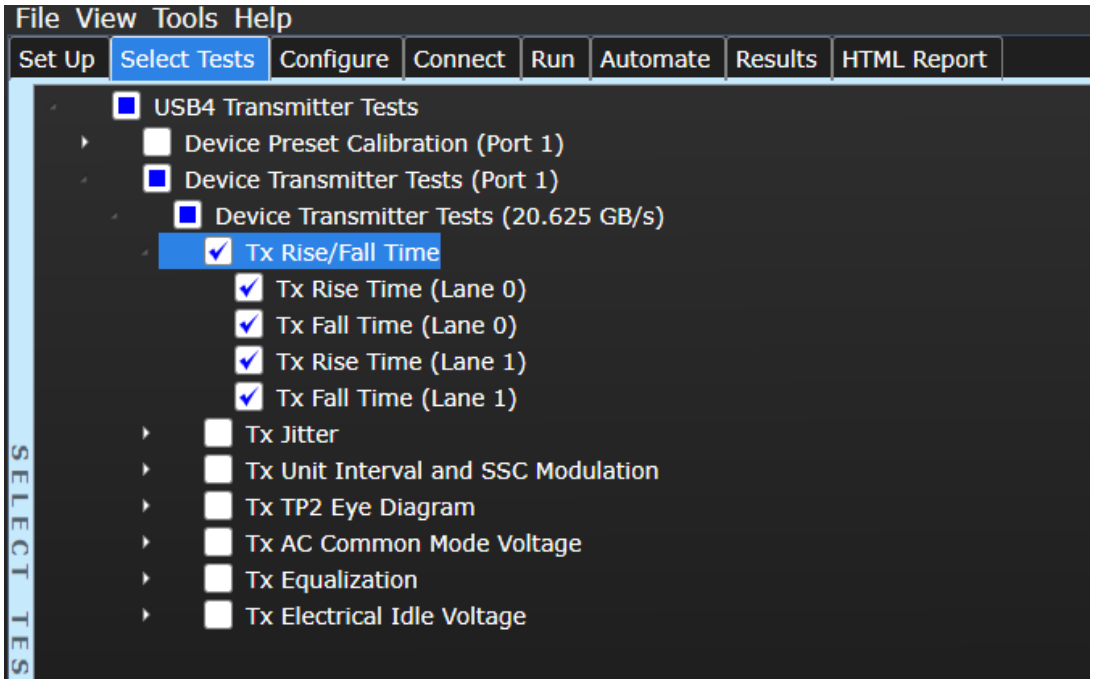


Figure 138 Selecting the Tx Rise/Fall Time tests

Test Procedure

1. Configure DUT transmitter to output alternating square pattern of 64 0's and 64 1's (SQ128) on all lanes with SSC turned on.
2. Evaluate at least 4Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ratio to 4Mpts. Use the maximum analog bandwidth of the Oscilloscope.

   No CDR, no average and no interpolation to be used.

   Adjust vertical scale such that the signal fits within the Oscilloscope's display.
3. Measure T_{RISE} as the mode of the sampled edge times from 20% to 80% of the differential swing voltage rising edge.
4. Measure T_{FALL} as the mode of the sampled edge times from 80% to 20% of the differential swing voltage falling edge.
5. Repeat the test for the remaining USB lanes.

Expected / Observable Results

If T_{RISE} < 10ps, the status of test is FAIL.

If T_{FALL} < 10ps, the status of test is FAIL.

Test References

See

- *USB4 Specification Version 2.00 (Table 3-2)*

Tx Uncorrelated Jitter

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Uncorrelated Jitter Test is to confirm that the Uncorrelated Jitter [Deterministic Jitter (DJ) and Random Jitter (RJ) components] of the transmitter is within the limits of the specification.

Test Pass Requirement

Uncorrelated Jitter (UJ) $\leq$ 0.31 UI_{p-p} (Refer to Table 8 on page 85).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 130 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter, Data Dependent Jitter and Duty Cycle Distortion* are checked.

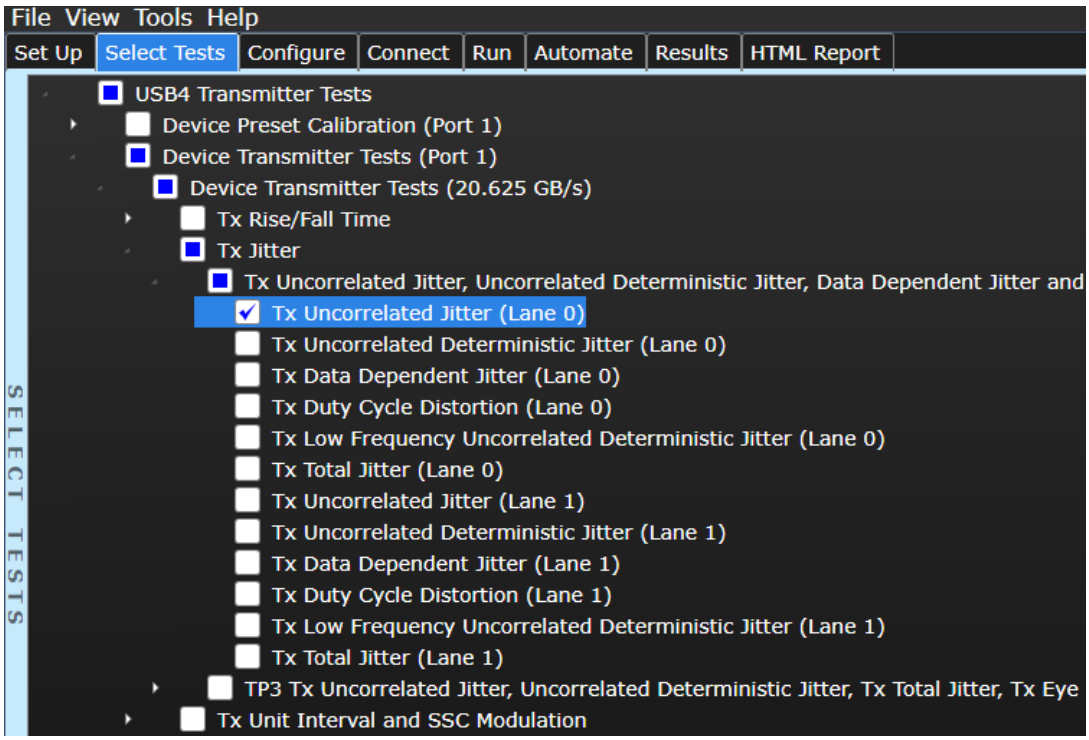


Figure 139 Selecting the Tx Uncorrelated Jitter tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2 Perform measurements with:
   a Reference CDR based on the 2^{nd} order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   b Oscilloscope with a minimum bandwidth of 21GHz
3 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Pattern length – Periodic
   c Jitter Separatio method must be suitable for cross-talk on the signal
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Evaluate 40 Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ratio to 40 Mpts
   f Referenced to 1E-13 statistics
4 Capture the Total Jitter (TJ) and Data Dependent Jitter (DDJ) results.
5 Calculate UJ using the equation:

$$UJ = TJ - DDJ$$

6 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If UJ > 0.31 UI_{p-p}, the status of test is FAIL.

Test References

See

- USB4 Specification Version 2.00 (Table 3-7)

Tx Uncorrelated Deterministic Jitter

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Uncorrelated Deterministic Jitter Test is to confirm that the Uncorrelated Deterministic Jitter of the transmitter is within the limits of the specification.

Test Pass Requirement

Uncorrelated Deterministic Jitter (UDJ) $\leq$ 0.17 UI_{p-p} (Refer to Table 8 on page 85).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 130 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the tests under the test group *Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter, Data Dependent Jitter and Duty Cycle Distortion* are checked.

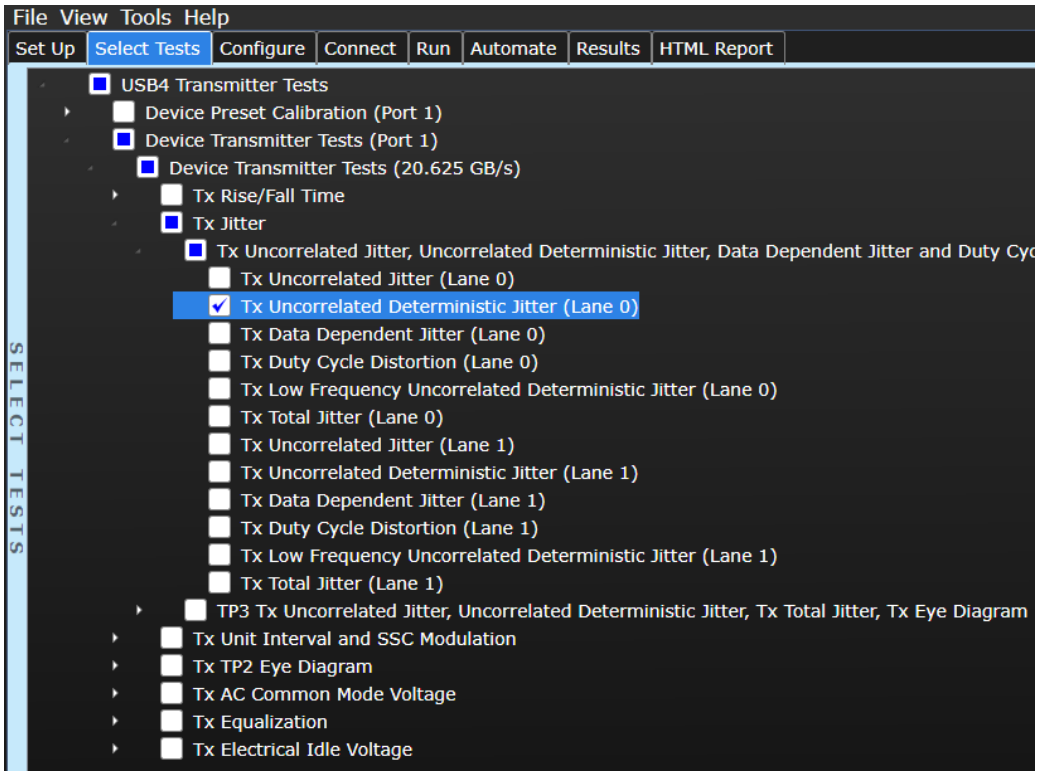


Figure 140 Selecting the Tx Uncorrelated Deterministic Jitter tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2 Perform measurements with:
   a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   b Oscilloscope with a minimum bandwidth of 21GHz
3 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Pattern length – Periodic
   c Jitter Separation method must be suitable for cross-talk on the signal
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Evaluate 40 Mpts per channel when using 80 GSa/s. For higher sample rates, use memory depth in the same ratio to 40 Mpts
   f Referenced to 1E-13 statistics
4 Capture the UDJ result (same as BUJ over the Oscilloscope).
5 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If UDJ > 0.17 UI_{p-p}, the status of test is FAIL.

Test References

See

- USB4 Specification Version 2.00 (Table 3-7)

Tx Data Dependent Jitter

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Data Dependent Jitter Test is to confirm that the sum of Data Dependent Jitter (DDJ) of a USB4 device must be less than the maximum limit as per the specification.

Test Pass Requirement

Data Dependent Jitter (DDJ) $\leq$ 0.21 UI_{p-p} (Refer to Table 8 on page 85).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 130 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter, Data Dependent Jitter and Duty Cycle Distortion* are selected.

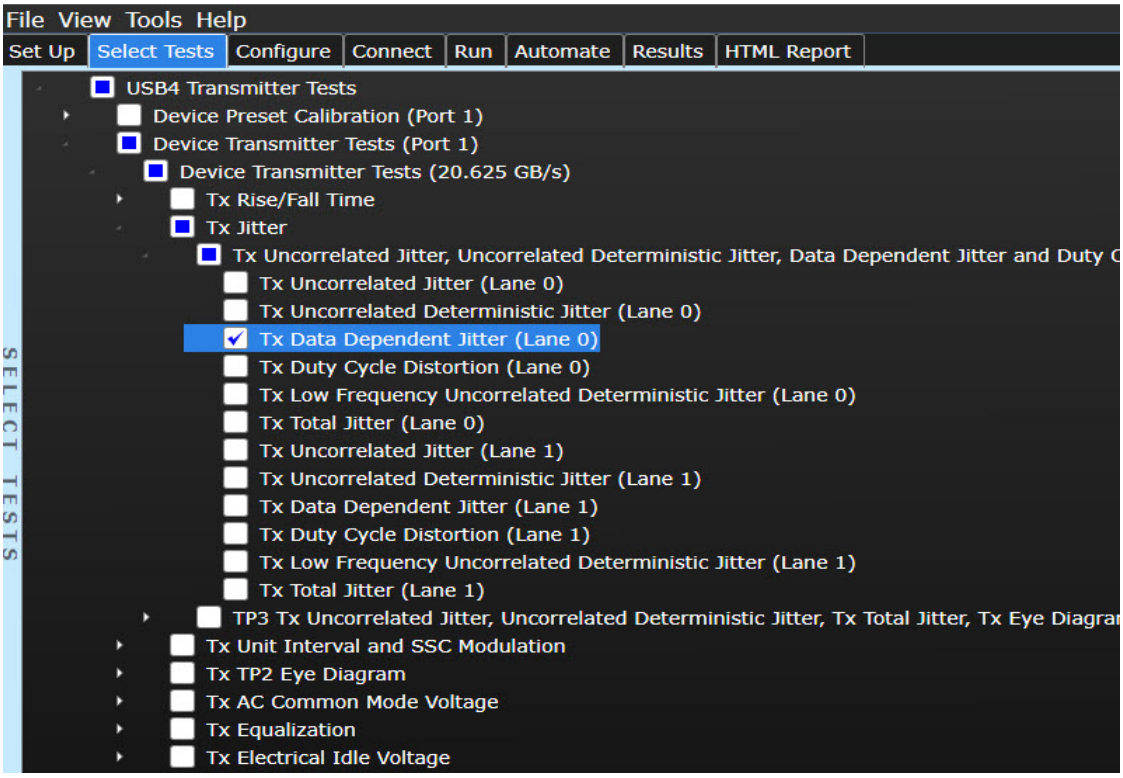


Figure 141 Selecting the Tx Data Dependent Jitter tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2 Perform measurements with:
   a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   b Oscilloscope with a minimum bandwidth of 21 GHz
3 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Pattern length – Periodic
   c Jitter Separation method must be suitable for cross-talk on the signal
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Evaluate 40 Mpts per channel when using 80 GSa/s. For higher sample rates, use memory depth in the same ratio to 40 Mpts
   f Referenced to 1E-13 statistics
4 Capture the DDJ result (same as ISI over the Oscilloscope).
5 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If DDJ > 0.21 UI_{p-p}, the status of test is FAIL.

Test References

See

- *USB4 Specification Version 2.00 (Table 3-7)*

Tx Duty Cycle Distortion

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Duty Cycle Distortion Test is to confirm that the transmitter Deterministic Jitter Associated by Duty-Cycle-Distortion Jitter falls within the limits of the specification.

Test Pass Requirement

Duty-Cycle-Distortion (DCD) ≤ 0.03 UIp-p (Refer to Table 8 on page 85).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 130 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter, Data Dependent Jitter and Duty Cycle Distortion* are checked.

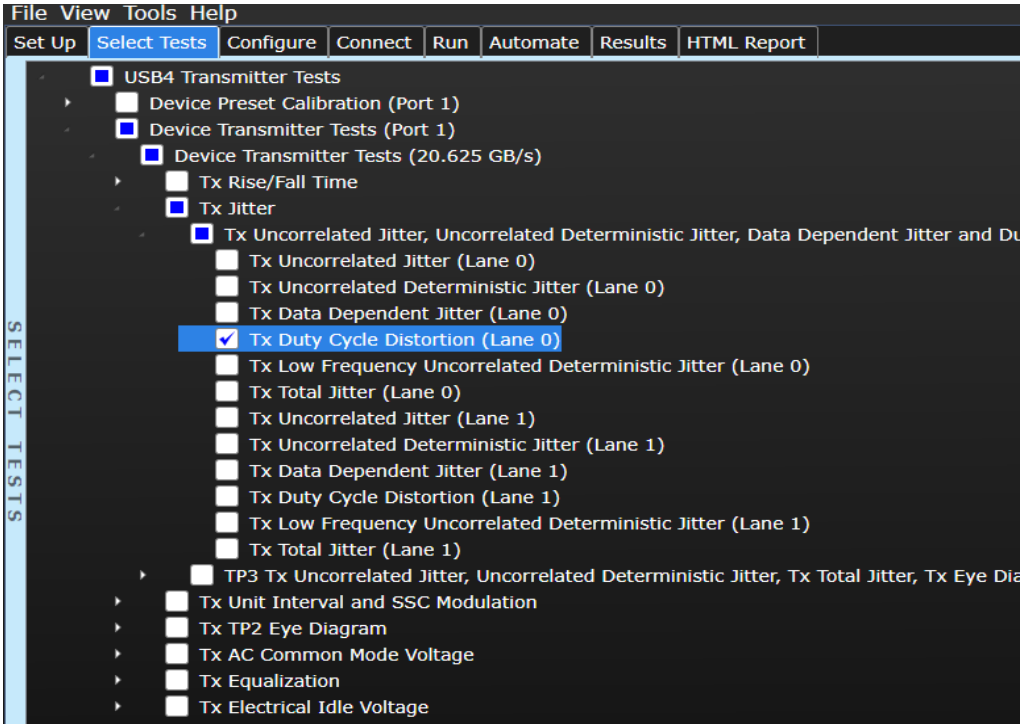


Figure 142 Selecting the Tx Duty Cycle Distortion tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2 Perform measurements with:
   a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   b Oscilloscope with a minimum bandwidth of 21GHz
3 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Pattern length – Periodic
   c Jitter Separatio method must be suitable for cross-talk on the signal
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Evaluate 40 Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ratio to 40 Mpts.
4 Capture the DCD result.
5 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If DCD > 0.03 UIp-p, the status of test is FAIL.

Test References

See

- *USB4 Specification Version 2.00 (Table 3-7)*

Tx Low Frequency Uncorrelated Deterministic Jitter

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Low Frequency Uncorrelated Deterministic Jitter Test is to confirm that the Low Frequency Uncorrelated Deterministic Jitter of the transmitter is within the limits of the specification.

Test Pass Requirement

Low Frequency Uncorrelated Deterministic Jitter (UDJ_LF) $\leq$ 0.07 UI_{p-p} (Refer to Table 8 on page 85).

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see Figure 130 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.
2. Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.
3. Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter, Data Dependent Jitter and Duty Cycle Distortion* are checked.

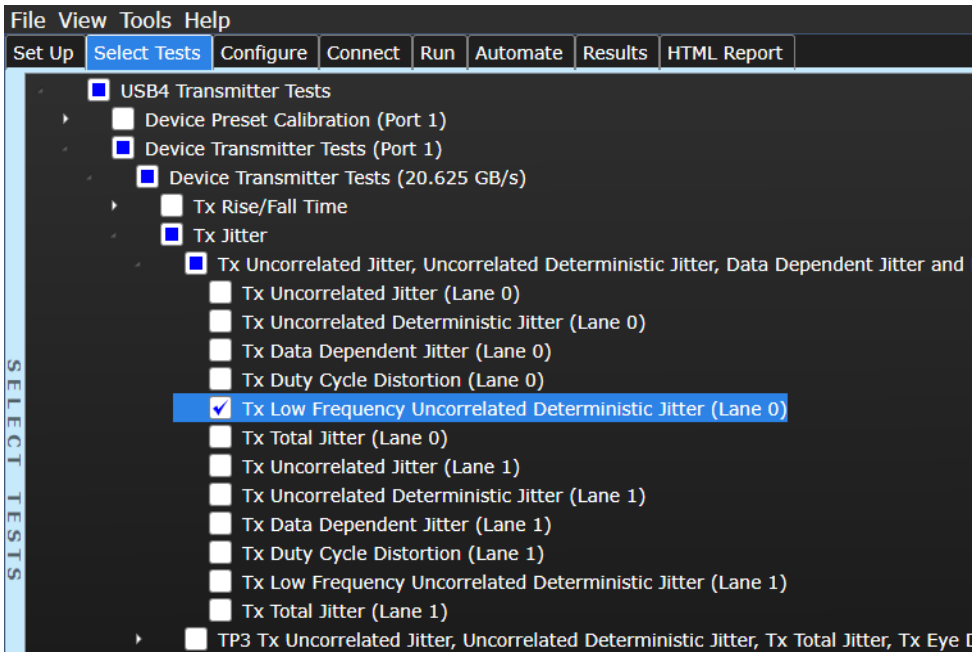


Figure 143 Selecting the Tx Low Frequency Uncorrelated Deterministic Jitter tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2 Perform measurements with:
   a Reference CDR based on the 2^{nd} order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 0.5 MHz and damping factor of 0.94
   b Apply 2^{nd} order Low-Pass-Filter with 3 dB cut-off at 2MHz; no average and no interpolation to be used
   c Oscilloscope with a minimum bandwidth of 21GHz
3 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Pattern length – Periodic
   c Jitter Separatio method must be suitable for cross-talk on the signal
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Evaluate 40 Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ratio to 40 Mpts
4 Capture the UDJ_LF result.
5 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If UDJ_LF > 0.07 UI_{p-p}, the status of test is FAIL.

Test References

See

USB4 Specification Version 2.00 (Table 3-7)

Tx Total Jitter

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Total Jitter Test is to confirm that the Total Jitter of the transmitter is within the limits of the specification.

Total Jitter (TJ) is defined as the sum of all “deterministic” components plus 14.7 times the Random Jitter (RJ) RMS. 14.7 is the factor that accommodates a Bit Error Ratio value of 1×10^{-13}.

Test Pass Requirement

Total Jitter (TJ) $\leq$ 0.46 UI_{p-p} (Refer to Table 8 on page 85).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 130 and for configuring the USB4 Test Application, see “Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to “Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Total Jitter* are checked.

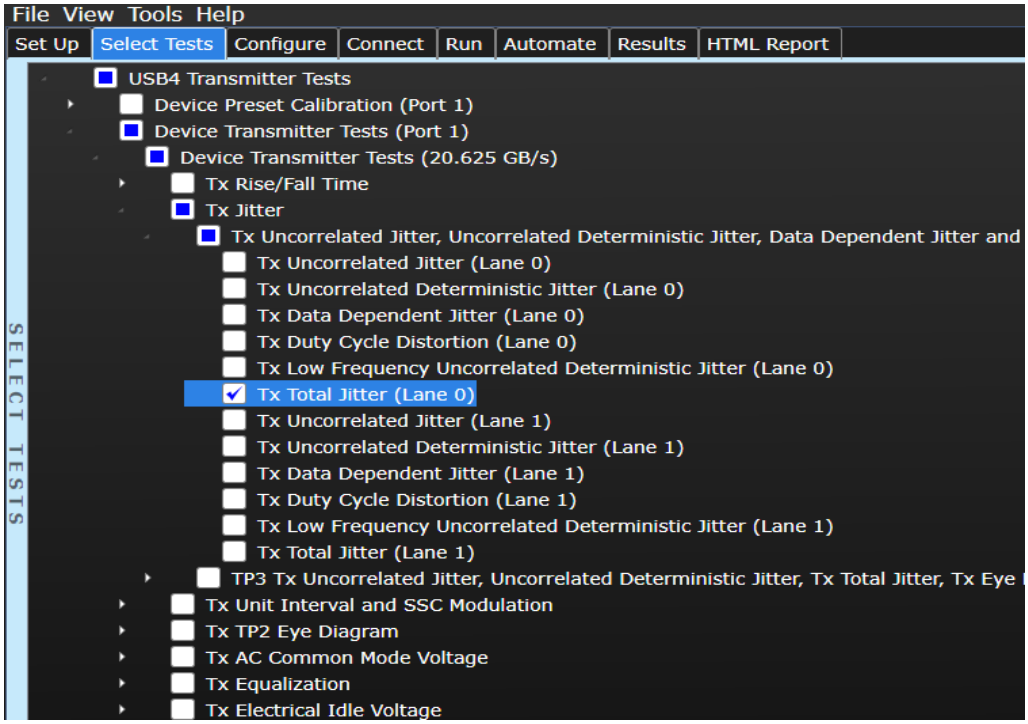


Figure 144 Selecting the Tx Total Jitter tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2 Perform measurements with:
   a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94
   b Oscilloscope with a minimum bandwidth of 21GHz
3 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Pattern length – Periodic
   c Jitter Separation method must be suitable for cross-talk on the signal
   d Evaluate 40 Mpts per channel when using 80 GSa/s. For higher sample rates, use memory depth in the same ratio to 40 Mpts
   e Adjust vertical scale such that the signal fits within the Oscilloscope's display.
   f Referenced to 1E-13 statistics.
4 Capture the values of Total Jitter (TJ) and Deterministic Jitter (DJ).
5 If TJ > 0.46 UI_{p-p}, perform the following steps:
   a Configure the DUT transmitter to output alternating square pattern of one 0's and one 1's on all lanes with SSC enabled. (The pattern is SQ2 instead of PRBS15).
   b Perform measurements with:
   - Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94
   - Oscilloscope with a minimum bandwidth of 21 GHz

   c Capture the waveform and process it with the Digital Oscilloscope:
   - Sampling Rate $\geq$ 80 GSa/s
   - Pattern length – Periodic
   - Jitter Separation method must be suitable for cross-talk on the signal
   - Evaluate 40 Mpts per channel when using 80 GSa/s. For higher sample rates, use memory depth in the same ratio to 40 Mpts
   - Adjust vertical scale such that the signal fits within the Oscilloscope's display.
   - Referenced to 1E-13 statistics.

   d Capture the Random Jitter (RJ) result.
   e Calculate TJ using the equation:

$$TJ = DJ + 14.7 * RJ \text{ (DJ from \#4; PRBS15 and RJ from \#5d; SQ2)}$$

6 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If TJ > 0.46 UI_{p-p}, the status of test is FAIL.

Test References

See

USB4 Specification Version 2.00 (Table 3-7)

Tx Uncorrelated Jitter TP3

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Uncorrelated Jitter TP3 Test is to confirm that the Uncorrelated Jitter [Deterministic Jitter (DJ) and Random Jitter (RJ) components] at point TP3 of the transmitter is within the limits of the specification.

Test Pass Requirement

Uncorrelated Jitter (UJ_{TP3}) $\leq$ 0.31 UI_{p-p} (Refer to Table 9 on page 86).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 130 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter, Data Dependent Jitter and Duty Cycle Distortion* are checked.

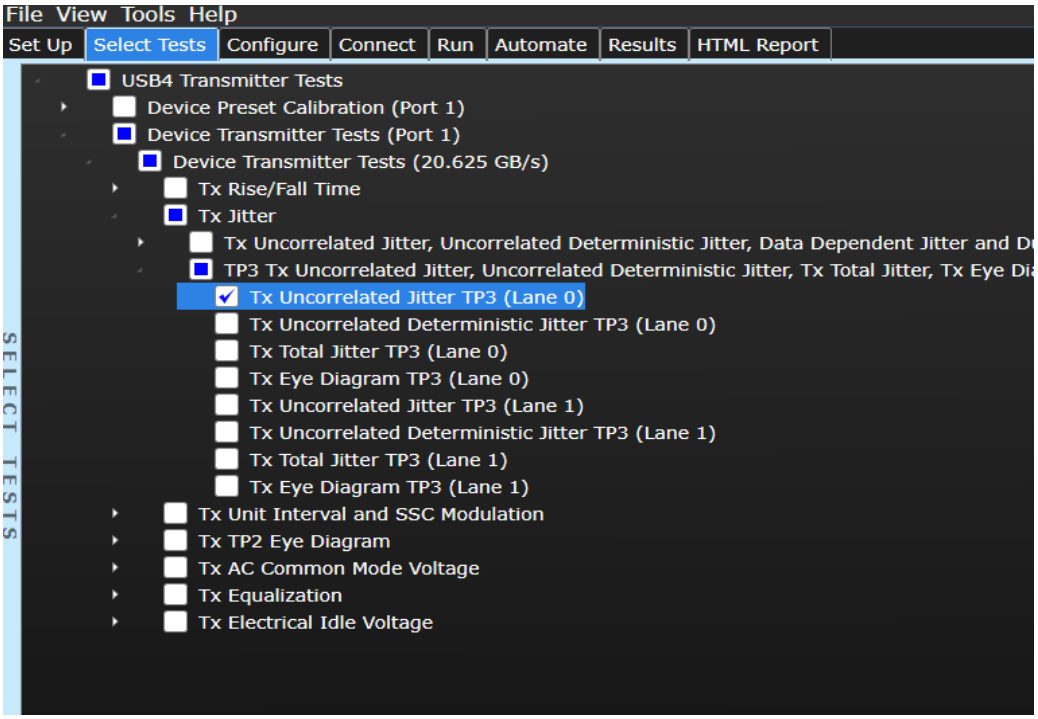


Figure 145 Selecting the Tx Uncorrelated Jitter TP3 tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2 Embed the Type-C cable in the Oscilloscope. For Gen 3 systems, use TP3_EQ embedding file *USB_0p8m.s4p*.
3 De-embed the cables from the test fixture to the Oscilloscope.
4 Perform measurements with:
   a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   b Oscilloscope with a minimum bandwidth of 21GHz
5 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Pattern length – Periodic
   c Jitter Separatio method must be suitable for cross-talk on the signal
   d Evaluate 40 Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ratio to 40 Mpts
   e Adjust vertical scale such that the signal fits within the Oscilloscope's display
   f Referenced to 1E-13 statistics
6 Capture the values of Total Jitter (TJ_{TP3}) and Data Deterministic Jitter (DDJ_{TP3}).
7 Calculate UJ_{TP3} using the equation:

$$UJ_{TP3} = TJ_{TP3} - DDJ_{TP3}$$

8 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If $UJ_{TP3} > 0.31\ UI_{p-p}$, the status of test is FAIL.

Test References

See

- *USB4 Specification Version 2.00 (Table 3-8)*

Tx Uncorrelated Deterministic Jitter TP3

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Sum of Uncorrelated Deterministic Jitter TP3 Test is to confirm that the sum of Uncorrelated Deterministic Jitter at point TP3 of the transmitter is within the limits of the specification.

Test Pass Requirement

Deterministic Jitter that is uncorrelated to the transmitted data (UDJ_{TP3}) $\leq$ 0.17 UI_{p-p} (Refer to Table 9 on page 86).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 130 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter, Data Dependent Jitter and Duty Cycle Distortion* are checked.

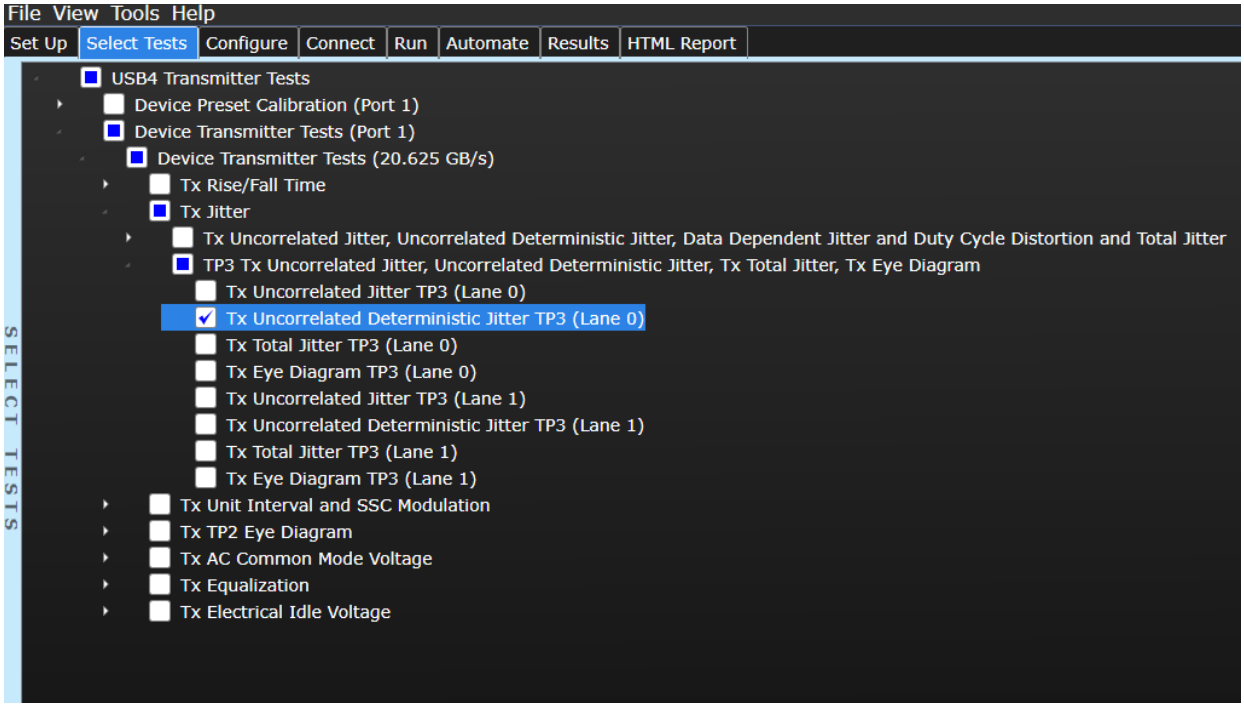


Figure 146 Selecting the Tx Uncorrelated Deterministic Jitter TP3 tests

Test Procedure

1. Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2. Embed the Type-C cable in the Oscilloscope. For Gen 3 systems, use TP3_EQ embedding file *USB_0p8m.s4p*.
3. De-embed the cables from the test fixture to the Oscilloscope.
4. Perform measurements with:
   a. Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   b. Oscilloscope with a minimum bandwidth of 21GHz
5. Capture the waveform and process it with the Digital Oscilloscope:
   a. Sampling Rate $\geq$ 80 GSa/s
   b. Pattern length – Periodic
   c. Jitter Separatio method must be suitable for cross-talk on the signal
   d. Evaluate 40 Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ratio to 40 Mpts
   e. Adjust vertical scale such that the signal fits within the Oscilloscope's display
6. Capture the values of Total Jitter (TJ_{TP3}) and Data Deterministic Jitter (DDJ_{TP3}).
7. Capture the UDJ_{TP3} result (same as BUJ over the Oscilloscope).
8. Repeat the test for the remaining USB lanes.

Expected / Observable Results

If $UDJ_{TP3} > 0.17\ UI_{p-p}$, the status of test is FAIL.

Test References

See

USB4 Specification Version 2.00 (Table 3-8)

Tx Total Jitter TP3

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Total Jitter TP3 Test is to confirm that the Total Jitter at point TP3 of the transmitter is within the limits of the specification.

Total Jitter (TJ) is defined as the sum of all “deterministic” components plus 14.7 times the Random Jitter (RJ) RMS. 14.7 is the factor that accommodates a Bit Error Ratio value of $1x10^{-13}$.

Test Pass Requirement

Total Jitter (TJ_{TP3}) $\leq$ 0.60 UI_{p-p} (Refer to Table 9 on page 86).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 130 and for configuring the USB4 Test Application, see “Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to “Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Total Jitter* are checked.

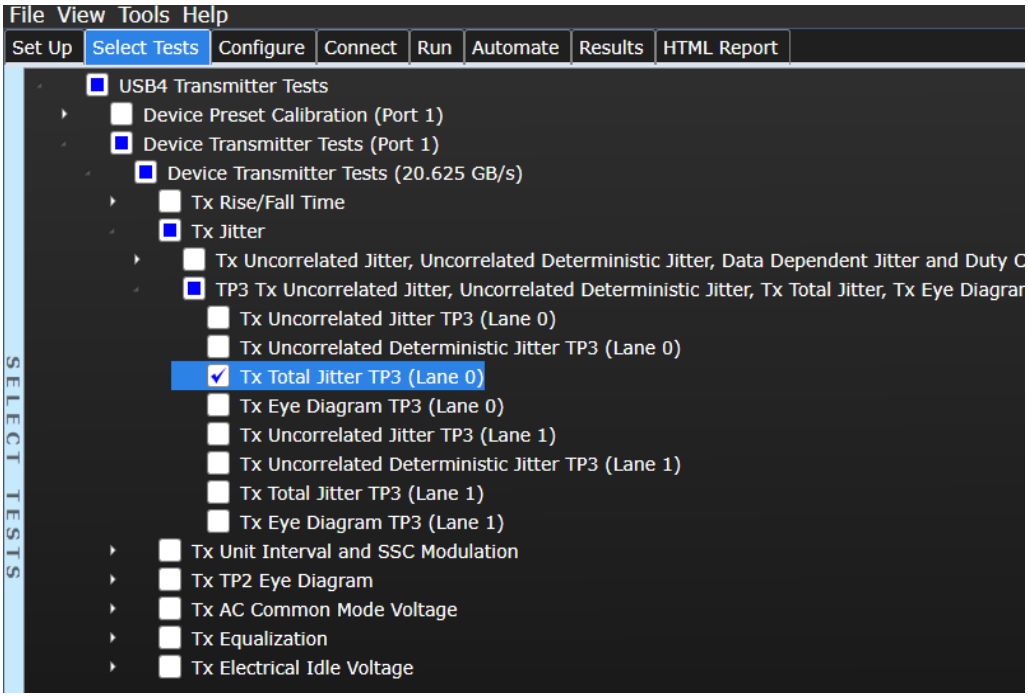


Figure 147 Selecting the Tx Total Jitter TP3 tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2 Embed the Type-C cable in the Oscilloscope. For Gen 3 systems, use TP3_EQ embedding file *USB_0p8m.s4p*.
3 De-embed the cables from the test fixture to the Oscilloscope.

NOTE CTLE value is handled in the SigTest tool.

4 Perform measurements with:
   a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   b Oscilloscope with a minimum bandwidth of 21GHz.
5 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Pattern length – Periodic
   c Jitter Separation method must be suitable for cross-talk on the signal
   d Evaluate 40 Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ratio to 40 Mpts
   e Adjust vertical scale such that the signal fits within the Oscilloscope's display
   f Referenced to 1E-13 statistics
6 Capture the values of Total Jitter (TJ_{TP3}) and Deterministic Jitter (DJ_{TP3}).
7 If $TJ_{TP3} > 0.60\ UI_{p-p}$, perform the following steps:
   a Configure the DUT transmitter to output alternating square pattern of one 0's and one 1's on all lanes with SSC enabled. (The pattern is SQ2 instead of PRBS15).
   b Perform measurements with:
   - Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94
   - Oscilloscope with a minimum bandwidth of 21GHz
   c Capture the waveform and process it with the Digital Oscilloscope:
   - Sampling Rate $\geq$ 80 GSa/s
   - Pattern length – Periodic
   - Jitter Separatio method must be suitable for cross-talk on the signal
   - Evaluate 40 Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ratio to 40 Mpts
   - Adjust vertical scale such that the signal fits within the Oscilloscope's display.
   - Referenced to 1E-13 statistics.
   d Capture the Random Jitter (RJ_{TP3}) result.
   e Calculate TJ_{TP3} using the equation:

$$TJ_{TP3} = DJ_{TP3} + 14.7 * RJ_{TP3}$$ (DJ_{TP3} from #7; PRBS15 and RJ_{TP3} from #8d; SQ2)

8 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If $TJ_{TP3} > 0.60\ UI_{p-p}$, the status of test is FAIL.

Test References

See

- USB4 Specification Version 2.00 (Table 3-8)

Tx Eye Diagram TP3

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Eye Diagram TP3 Test is to confirm that the differential signal on each USB differential lane has an eye opening that meets or exceeds the limits for eye opening in the specification.

Test Pass Requirement

The eye diagram at TP3 should meet the conditions depicted in Figure 148.

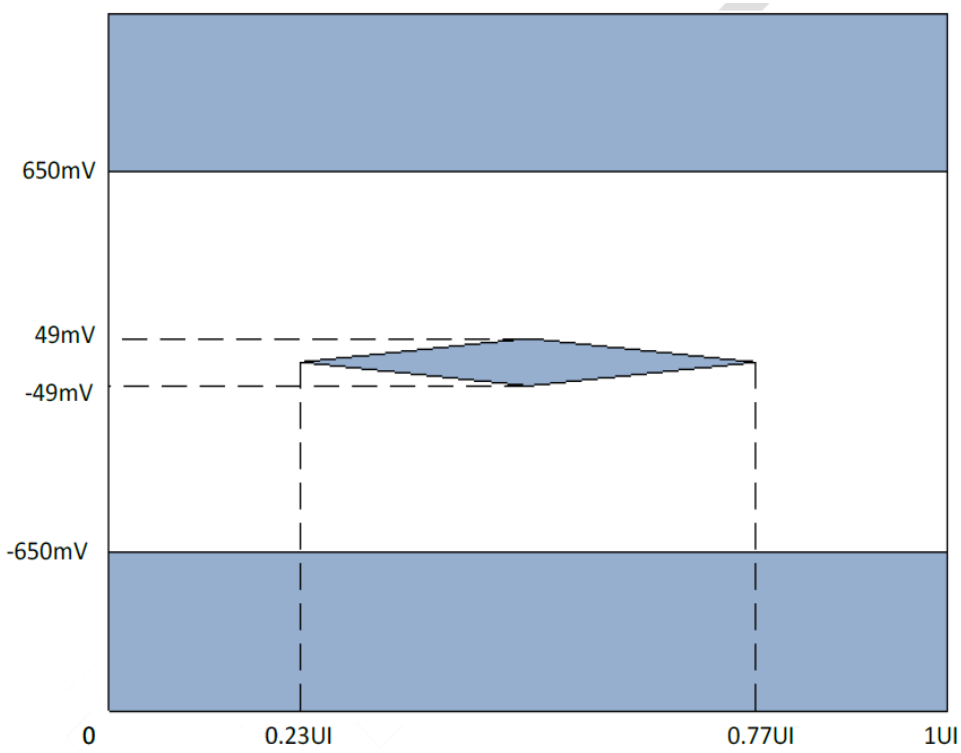


Figure 148 Pass Condition for Tx Eye Diagram TP3 Tests

(Refer to Table 9 on page 86 and Figure 148 on page 300).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter TP2/TP3 Test Setup" on page 264 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Eye Diagram* are checked.

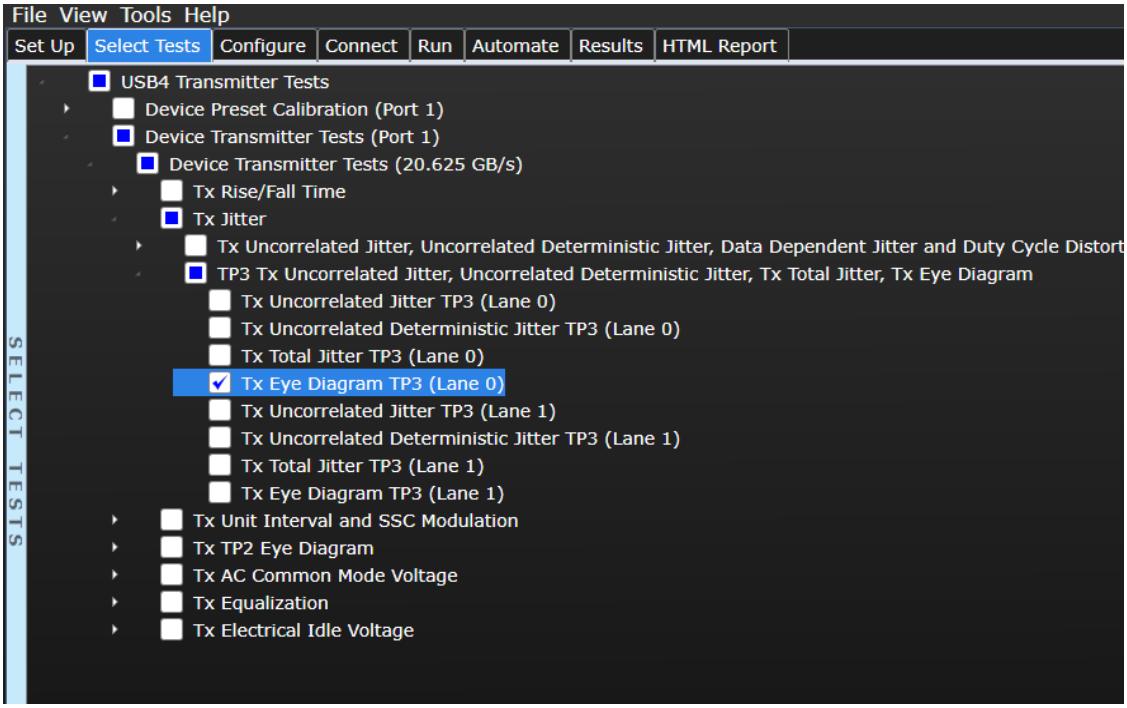


Figure 149 Selecting the Tx Eye Diagram TP3 tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2 Embed the Type-C cable in the Oscilloscope. For Gen 3 systems, use TP3_EQ embedding file *USB_0p8m.s4p*.
3 De-embed the cables from the test fixture to the Oscilloscope.

NOTE CTLE and DFE values are handled in the SigTest tool.

4 Perform measurements with:
   a Change from no interpolation to X16 a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and X16 interpolation to be used.
   b Oscilloscope with a minimum bandwidth of 21GHz
5 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Adjust vertical and horizontal scale such that the signal fits within the Oscilloscope's display
   c Accumulate at 1E6 UI
6 Compare the data eye to the TP3 eye diagram mask. Check for conditions described in the section "Expected / Observable Results".

7 Repeat the test for the remaining USB lanes.

Expected / Observable Results

i If any part of the waveform exceeds either the high or low maximum voltage (+/-1000mV), the status of the test is FAIL.

ii If any part of the waveform hits the mask, the status of the test is FAIL.

Test References

See

- *USB4 Specification Version 2.00 (Table 3-8)*

Tx Minimum Unit Interval Min/Max

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Unit Interval Test is to confirm that the data rate, under all conditions, does not exceed the minimum or maximum limits of the specification.

Test Pass Requirement

Tx Minimum Unit Interval Min

Minimum Unit Interval, Min (Device, 20.625 Gb/s) >= 48.4703 ps

Tx Minimum Unit Interval Max

Minimum Unit Interval, Max (Device, 20.625 Gb/s) <= 48.4994 ps

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 130 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Unit Interval and SSC Down Spread Modulation* are checked.

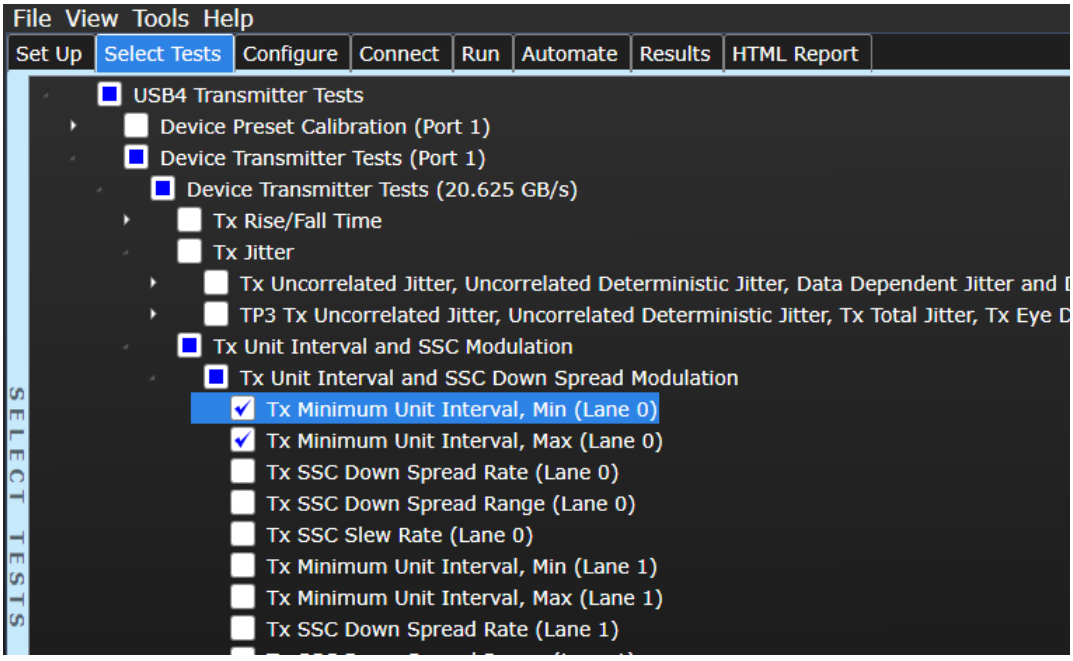


Figure 150 Selecting the Tx Unit Interval tests

Test Procedure

1. Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2. Capture the waveform and process it with the Digital Oscilloscope:
   - *a* Sampling Rate $\geq$ 80 GSa/s
   - *b* Evaluate 27Mpts per channel when using 80 GSa/s. For higher sample rates, use memory depth in the same ratio to 27 Mpts
   - *c* No CDR, no average and no interpolation to be used
   - *d* Adjust vertical scale such that the signal fits within the Oscilloscope's display
   - *e* Oscilloscope must have a minimum bandwidth of 21 GHz
3. Calculate UI dynamically using a uniform moving average filter procedure with a window size of 6000 symbols.
4. Measure the values of both UI_{MAX} and UI_{MIN}.
5. Repeat the test for the remaining USB lanes.

Expected / Observable Results

If UI_{MAX} > 48.4994 ps, the status of test is FAIL.

If UI_{MIN} < 48.4703 ps, the status of test is FAIL.

Test References

See

- *USB4 Specification Version 2.00 (Table 13-1)*

Tx SSC Down Spread Rate

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx SSC Down Spread Rate Test is to confirm that the Link clock down-spreading modulation rate is within the limits of the specification.

Test Pass Requirement

30.000 kHz ≤ SSC_Down_Spread_Rate ≤ 37.000 kHz (Refer to Table 3 on page 74).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 130 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Unit Interval and SSC Down Spread Modulation* are checked.

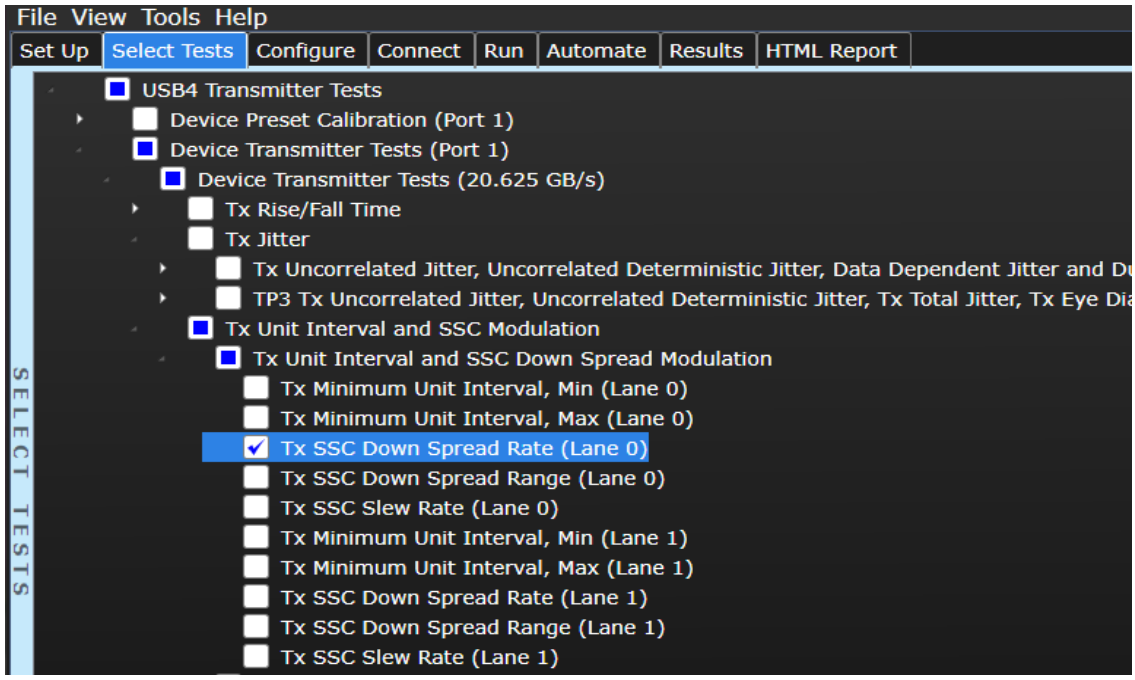


Figure 151 Selecting the Tx SSC Down Spread Rate tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Evaluate 27 Mpts per channel when using 80 GSa/s. For higher sample rates, use memory depth in the same ratio to 27 Mpts
   c No CDR, no average and no interpolation to be used
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Oscilloscope must have a minimum bandwidth of 21 GHz
3 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If 30.000 kHz > SSC_Down_Spread_Rate > 37.000 kHz, the status of test is FAIL.

Test References

See

- *USB4 Specification Version 2.00 (Table 13-1)*

Tx SSC Down Spread Range

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx SSC Down Spread Range Test is to confirm that the data down spreading is within the limits of the specification.

Test Pass Requirement

0.4% ≤ SSC_Down_Spread_Range ≤ 0.5% (Refer to Table 3 on page 74).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 130 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Unit Interval and SSC Down Spread Modulation* are checked.

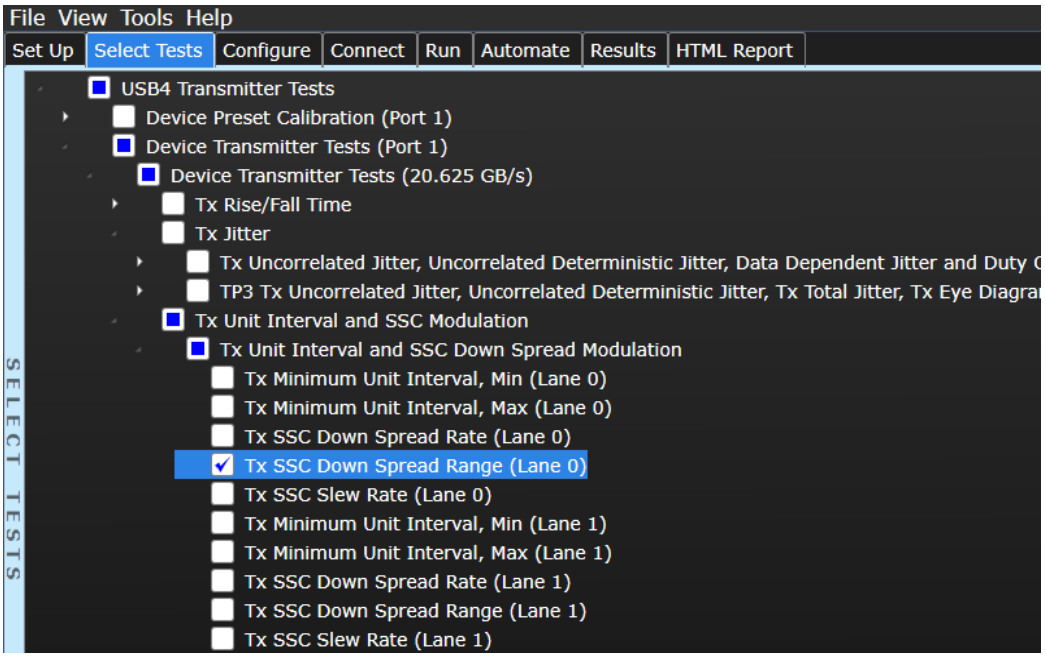


Figure 152 Selecting the Tx SSC Down Spread Range tests

Test Procedure

1. Run the "Tx Eye Diagram TP3" Test as a prerequisite to obtain UI_{MAX} and UI_{MIN}.
2. Use the obtained value of UI_{MAX} and UI_{MIN} to calculate the Deviation percentage:

$$\text{Maximum Deviation} = 100*\{[20.625G - (1 / UI_{MAX})] / 20.625G\}$$

$$\text{Minimum Deviation} = 100*\{[20.625G - (1 / UI_{MIN})] / 20.625G\}$$

3. Calculate SSC Down Spread Range using the equation:

$$\text{Maximum Deviation - Minimum Deviation}$$

4. Repeat the test for all remaining USB lanes.

Expected / Observable Results

If SSC_Down_Spread_Range > 0.5% or SSC_Down_Spread_Range < 0.4%, the status of test is FAIL.

Test References

See

USB4 Specification Version 2.00 (Table 3-2)

Tx SSC Slew Rate

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx SSC Slew Rate Test is to confirm that the SSC Slew Rate is within the limits of the specification.

Test Pass Requirement

SSC_Slew_Rate $\leq$ 1250 ppm/µs (Refer to Table 3 on page 74).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 130 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Unit Interval and SSC Down Spread Modulation* are checked.

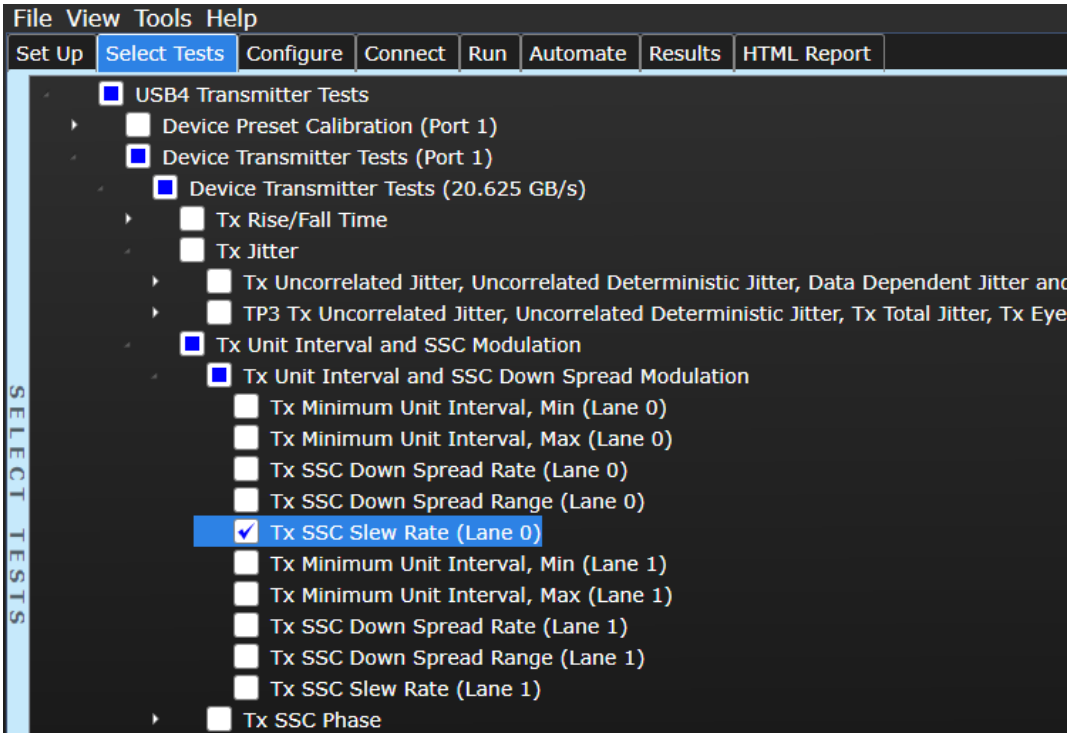


Figure 153 Selecting the Tx SSC Slew Rate tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2 Capture the waveform and post process it with an appropriate software:
   a Sampling Rate $\geq$ 80 GSa/s
   b Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ratio to 27Mpts
   c No CDR, no average and no interpolation to be used
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Extract SSC slew rate from the transmitted signal over measurement intervals of 0.5µs
   f Extract SSC slew rate from the phase information after applying a 2^{nd} order Low-Pass-Filter with 3 dB cut-off at 5 MHz.
   g Oscilloscope must have a minimum bandwidth of 21GHz
3 SSC_Slew_Rate is measured as the SSC frequency deviation over time while valid data is being transmitted in which 1E-12 bit error rate is required without assuming forward error correction.
4 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If SSC_Slew_Rate_Data > 1250 ppm/µs, the status of test is FAIL.

Test References

See

USB4 Specification Version 2.00 (Table 3-2)

Tx SSC Phase Deviation

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx SSC Phase Deviation Test is to confirm that the SSC Phase Deviation is within the limits of the specification.

Test Pass Requirement

2.50 ns p-p ≤ SSC_Phase_Deviation ≤ 22.00 ns p-p (Refer to Table 3 on page 74).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 130 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx SSC Phase* are checked.

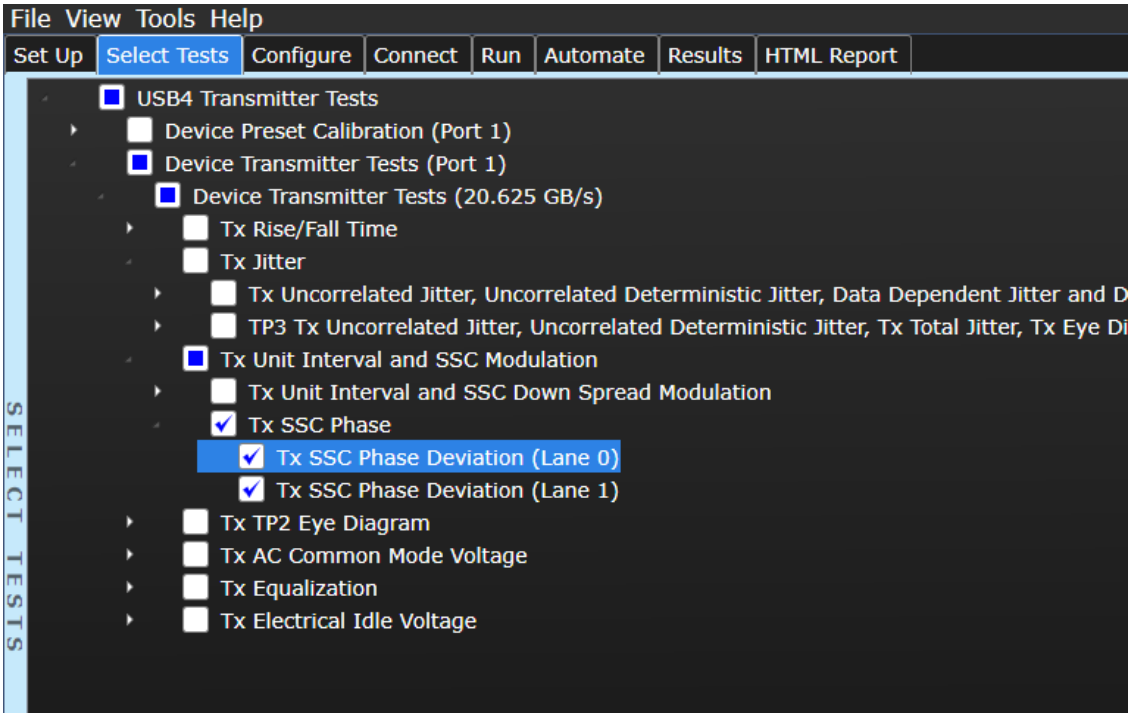


Figure 154 Selecting the Tx SSC Phase Deviation tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2 Capture the waveform and process it with the Digital Oscilloscope's software:
   a Sampling Rate $\geq$ 80 GSa/s
   b Evaluate 27 Mpts per channel when using 80 GSa/s. For higher sample rates, use memory depth in the same ratio to 27 Mpts
   c No CDR, no average and no interpolation to be used
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Oscilloscope must have a minimum bandwidth of 21 GHz
3 Extract the SSC Phase Deviation from the transmitted signal.
4 Extract the SSC Phase Deviation from the phase jitter after applying a 2^{nd} order low-pass filter with 3 dB point at 5 MHz.
5 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If 2.50 ns p-p > SSC_Phase_Deviation > 22.00 ns p-p the status of test is FAIL.

Test References

See

USB4 Specification Version 2.00 (Table 13-1)

Tx Eye Diagram

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Eye Diagram Test is to confirm that the differential signal on each USB differential lane has an eye opening that meets or exceeds the limits for eye opening in the specification.

Test Pass Requirement

The eye diagram should meet the conditions depicted in Figure 155.

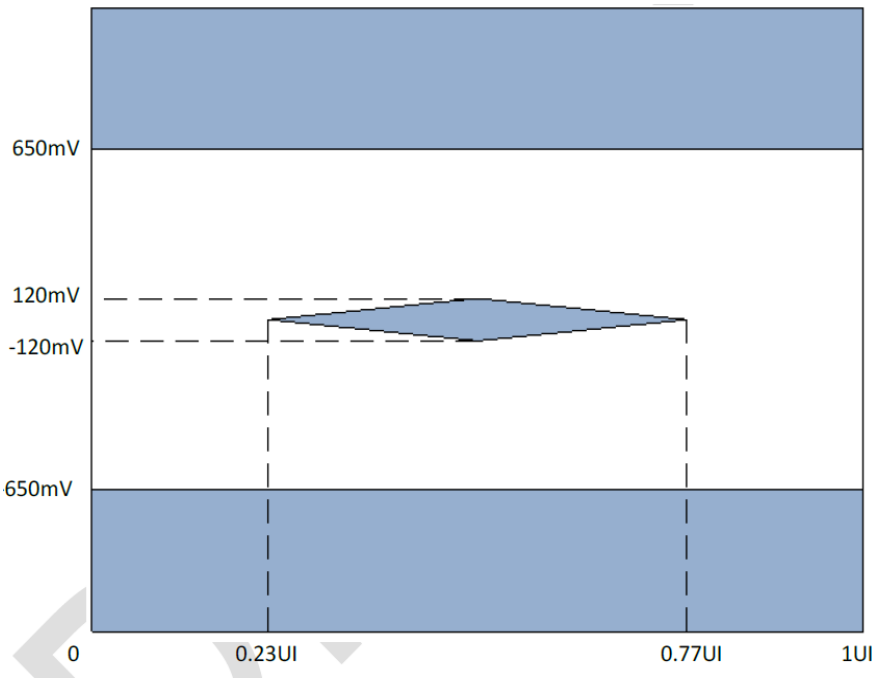


Figure 155 Pass Condition for Tx Eye Diagram Tests

(Refer to Table 8 on page 85 and Figure 155 on page 313).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter TP2/TP3 Test Setup" on page 264 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Eye Diagram* are checked.

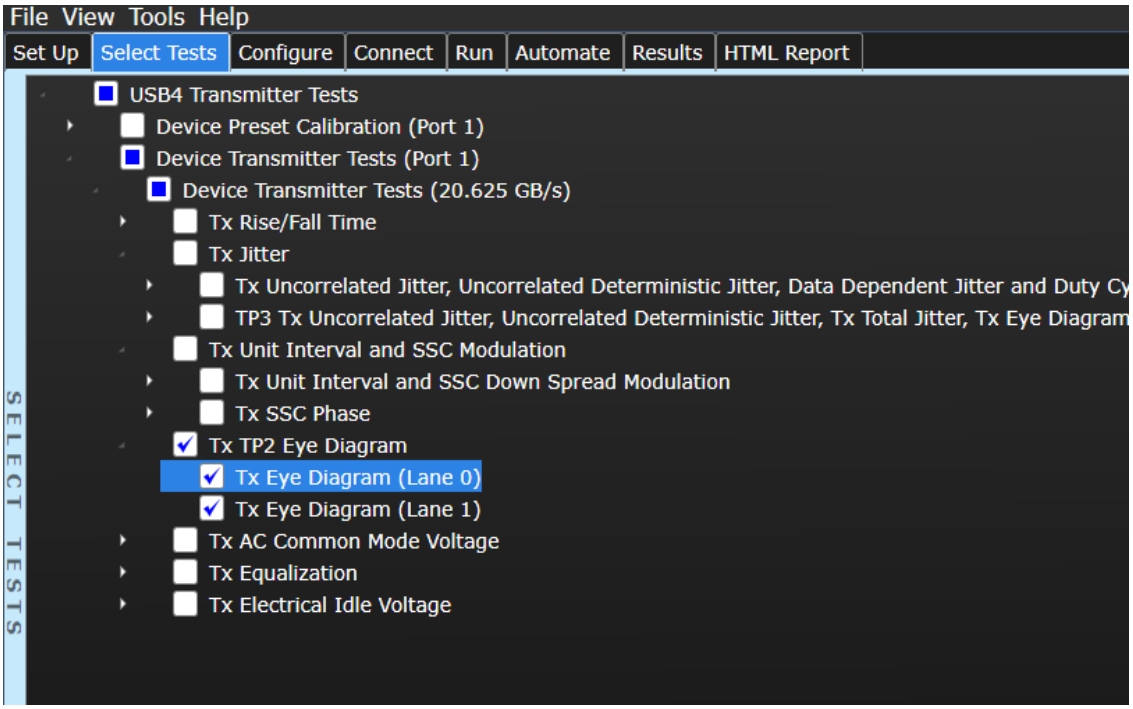


Figure 156 Selecting the Tx Eye Diagram tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2 Perform measurements with:
   a Perform measurements with: Change from no interpolation to X16 a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and X16 interpolation to be used.
   b Oscilloscope with a minimum bandwidth of 21GHz
3 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Adjust vertical scale such that the signal fits within the Oscilloscope's display
   c Measured at 1E6 UI
4 Compare the data eye to the TP1 eye diagram mask. Check for conditions described in the section "Expected / Observable Results".
5 Repeat the test for the remaining USB lanes.

Expected / Observable Results

i If any part of the waveform exceeds either the inner or outer height voltage (+/- 700mV), the status of the test is FAIL.
ii If any part of the waveform hits the mask, the status of the test is FAIL.

Test References

See

- USB4 Specification Version 2.00 (Table 3-7)

Tx AC Common Mode Voltage

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx AC Common Mode Voltage Test is to confirm that the transmitter common mode on the USB differential signals is within the limits of the specification.

Test Pass Requirement

TX AC Common Mode Voltage $\leq$ 100 mV_{p-p} (Refer to Table 8 on page 85).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 130 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx AC Common Mode Voltage* are checked.

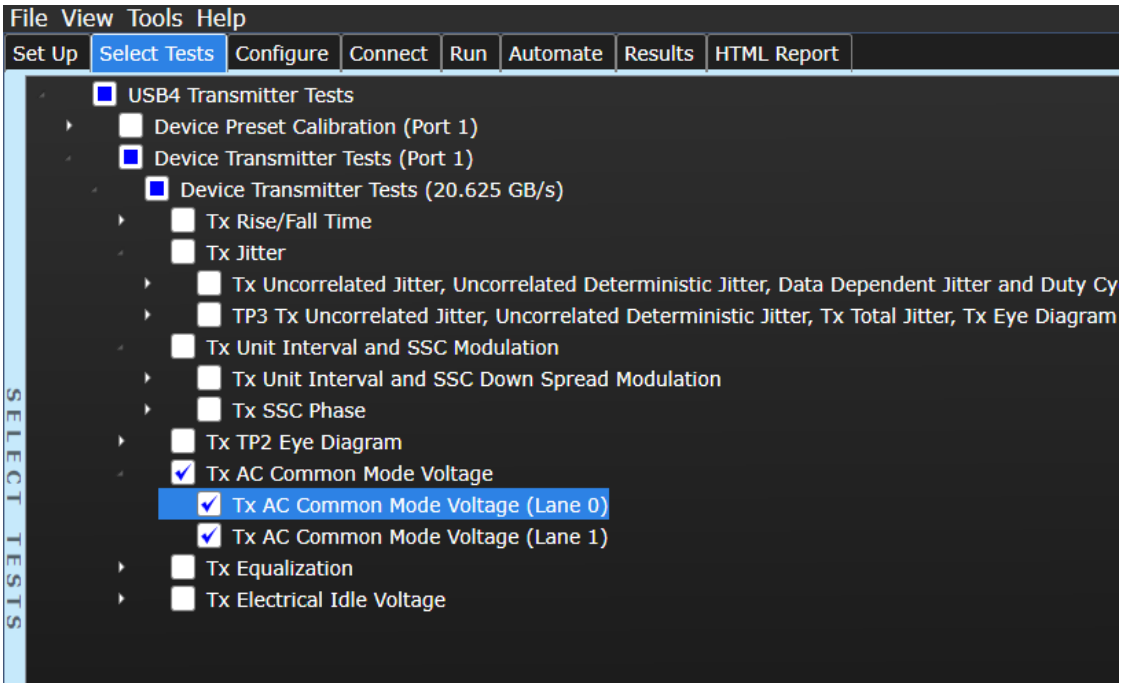


Figure 157 Selecting the Tx AC Common Mode Voltage tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ratio to 27Mpts
   c No CDR, no average and no interpolation to be used
   d Oscilloscope must have a minimum bandwidth of 21GHz
3 Calculate the AC Common Mode Voltage (V_{AC-CM}) using the equation:

$$V_{AC-CM} = (V_{TX-P} + V_{TX-N}) / 2$$

4 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If $V_{AC-CM} > 100\ mV_{p-p}$, the status of test is FAIL.

Test References

See,

USB4 Specification Version 2.00 (Table 3-7)

Tx Equalization Tests

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Equalization Tests is to confirm that the transmitter equalization is within the limits of the specification. The Tx Equalization Tests are further divided into three tests, namely:

- Tx Equalization Preshoot
- Tx Equalization Deemphasis
- Tx Swing Preset 15

Test Pass Requirement

Transmitter Swing: 3.5 ± 1dB (for preset 15 only)

Preshoot, De-Emphasis: ± 1dB for the following presets:

Table 12 Transmitter Equalization Presets

Preset Number	Pre-Shoot	De-Emphasis	Informative Filter Coefficients		
			C_{-1}	C_0	C_1
0	0	0	0	1	0
1	0	-1.9	0	0.90	-0.10
2	0	-3.6	0	0.83	-0.17
3	0	-5.0	0	0.78	-0.22
4	0	-8.4	0	0.69	-0.31
5	0.9	0	-0.05	0.95	0
6	1.1	-1.9	-0.05	0.86	-0.09
7	1.4	-3.8	-0.05	0.79	-0.16
8	1.7	-5.8	-0.05	0.73	-0.22
9	2.1	-8.0	-0.05	0.68	-0.27
10	1.7	0	-0.09	0.91	0
11	2.2	-2.2	-0.09	0.82	-0.09
12	2.5	-3.6	-0.09	0.77	-0.14
13	3.4	-6.7	-0.09	0.69	-0.22
14	3.6	0	-0.17	0.83	0
15	1.7	-1.7	-0.05	0.55	-0.05

(Refer to Table 5 on page 81).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 130 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Equalization* are checked.

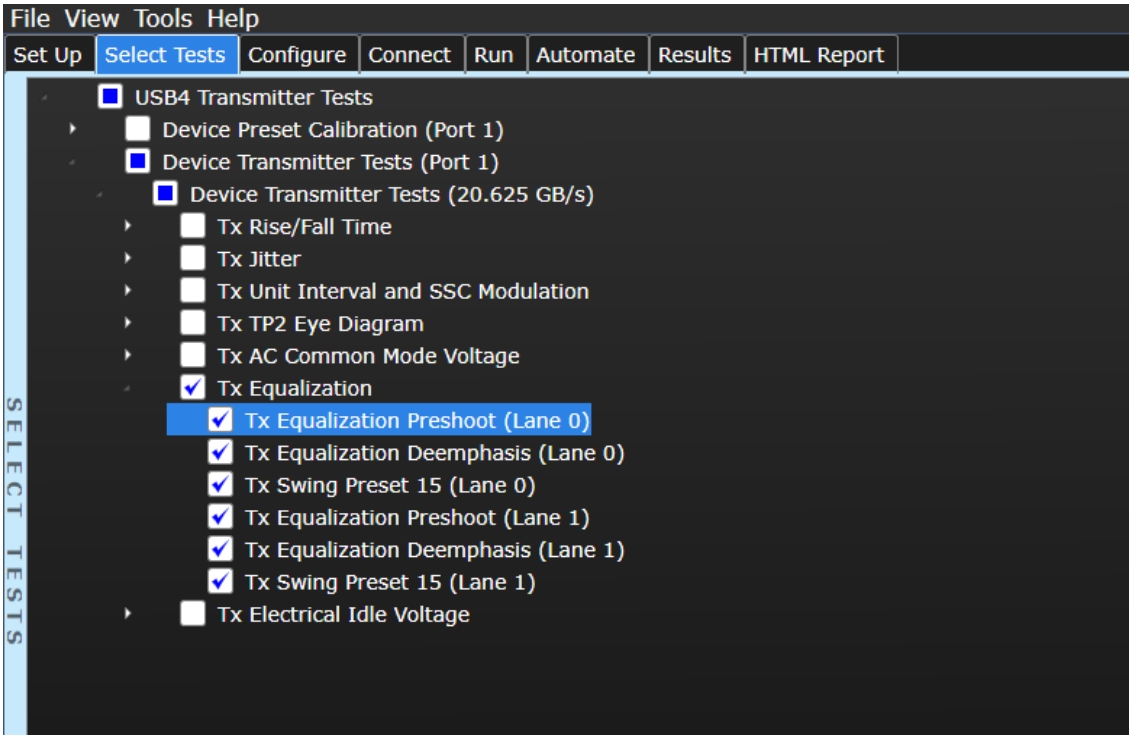


Figure 158 Selecting the Tx Equalization tests

4 Under the **Configure** tab of the Test Application, select **ALL** for the configuration Variable “Tx Equalization” to run the tests for preset numbers P0 to P15.

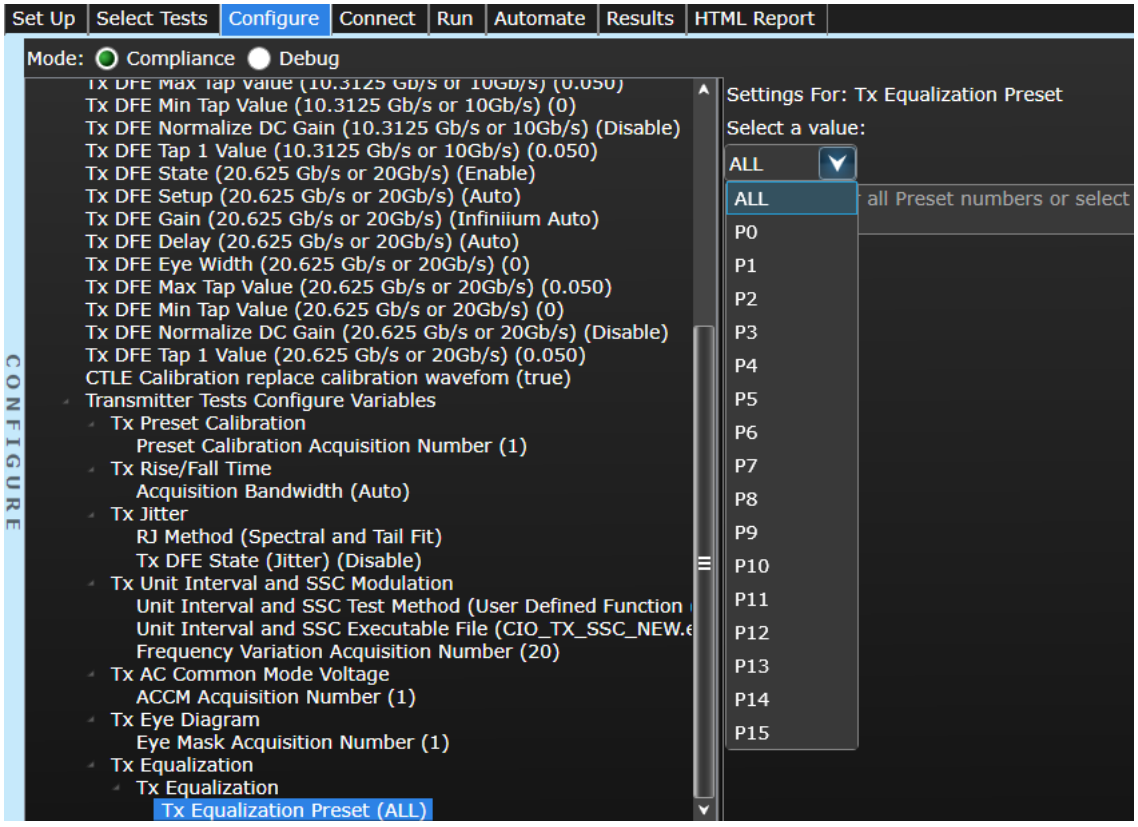


Figure 159 Configuring Tx Equalization Preset Variable

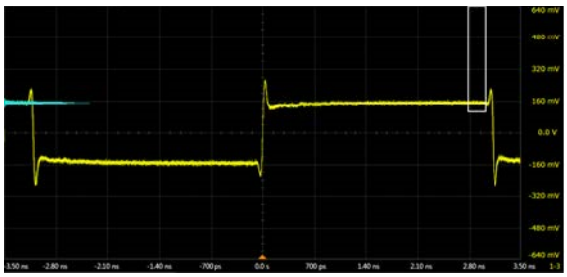
Test Procedure

1 Set Preset 0 (P0).

2 Configure the DUT transmitter to output alternating square pattern of 64 0’s and 64 1’s on all lanes with SSC enabled along with both pre-shoot and de-emphasis enabled.

3 Adjust vertical scale such that the signal fits within the Oscilloscope’s display.

4 Average one cycle using 150 cycles; no CDR and no interpolation to be used. Oscilloscope must have a minimum bandwidth of 21GHz.



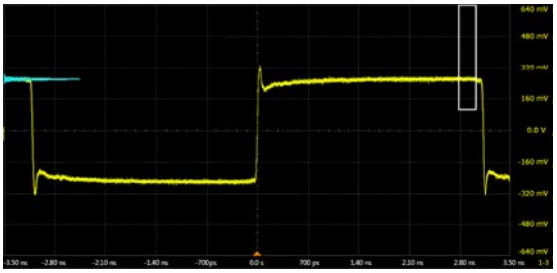
5 Measure differential amplitude voltage (V_1) for bits 57 to 62 using the equation:

$$V_1 = [|V_{bits(57\text{-}62)} \text{ (64 bits of 1's)} - V_{bits(57\text{-}62)} \text{ (64 bits of 0's)}|]$$

6 Configure the DUT transmitter to output alternating square pattern of 64 0's and 64 1's on all lanes with SSC enabled along with de-emphasis enabled but no pre-shoot.

7 Adjust vertical scale such that the signal fits within the Oscilloscope's display.

8 Average one cycle using 150 cycles; no CDR and no interpolation to be used. Oscilloscope must have a minimum bandwidth of 21GHz.



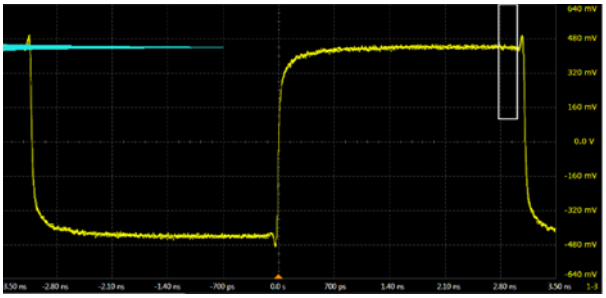
9 Measure differential amplitude voltage (V_2) for bits 57 to 62 using the equation:

$$V_2 = [|V_{bits(57\text{-}62)} \text{ (64 bits of 1's)} - V_{bits(57\text{-}62)} \text{ (64 bits of 0's)}|]$$

10 Configure the DUT transmitter to output alternating square pattern of 64 0's and 64 1's on all lanes with SSC enabled along with pre-shoot enabled but no de-emphasis.

11 Adjust vertical scale such that the signal fits within the Oscilloscope's display.

12 Average one cycle using 150 cycles; no CDR and no interpolation to be used. Oscilloscope must have a minimum bandwidth of 21GHz.



13 Measure differential amplitude voltage (V_3) for bits 57 to 62 using the equation:

$$V_3 = [|V_{bits(57\text{-}62)} \text{ (64 bits of 1's)} - V_{bits(57\text{-}62)} \text{ (64 bits of 0's)}|]$$

$$\text{Set Pre-Shoot to be } 20 * \log_{10}[V_2/V_1]$$

$$\text{Set De-Emphasis to be } 20 * \log_{10}[V_1/V_3]$$

14 Repeat steps 2 to 10 for all Presets defined in Table 12.

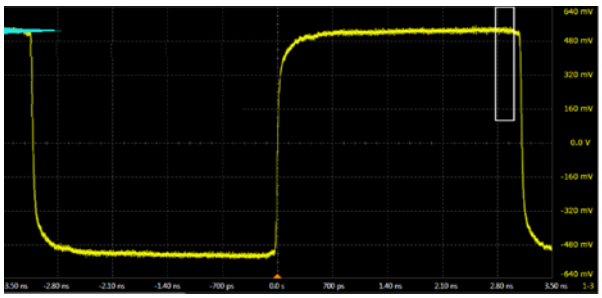
15 Check for PASS/FAIL conditions for both Pre-shoot and De-emphasis.

16 Set the DUT to Preset 0 (P0).

17 Configure the DUT transmitter to output alternating square pattern of 64 0's and 64 1's on all lanes with SSC enabled but with both pre-shoot and de-emphasis disabled.

18 Adjust vertical scale such that the signal fits within the Oscilloscope's display.

19 Average one cycle using 150 cycles; no CDR and no interpolation to be used. Oscilloscope must have a minimum bandwidth of 21GHz.



20 Measure differential amplitude voltage (V_0) for bits 57 to 62 using the equation:

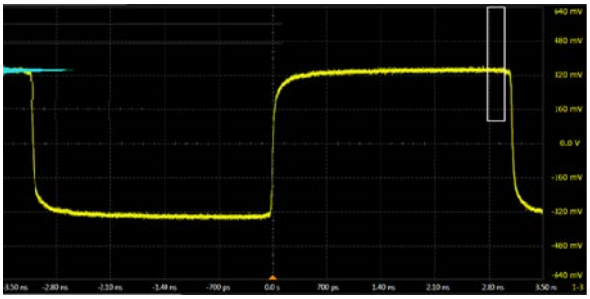
$$V_0 = [|V_{bits(57-62)} \text{ (64 bits of 1's)} - V_{bits(57-62)} \text{ (64 bits of 0's)}|]$$

21 Set the DUT to Preset 15 (P15).

22 Configure the DUT transmitter to output alternating square pattern of 64 0's and 64 1's on all lanes with SSC enabled but with both pre-shoot and de-emphasis disabled.

23 Adjust vertical scale such that the signal fits within the Oscilloscope's display.

24 Average one cycle using 150 cycles; no CDR and no interpolation to be used. Oscilloscope must have a minimum bandwidth of 21GHz.



25 Measure differential amplitude voltage (V_{15}) for bits 57 to 62 using the equation:

$$V_{15} = [|V_{bits(57-62)} \text{ (64 bits of 1's)} - V_{bits(57-62)} \text{ (64 bits of 0's)}|]$$

Set Swing to be $20 * \log_{10} [V_0/V_{15}]$

26 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If the Pre-Shoot for a particular Preset number is not within ± 1dB of the matching value in Table 12, the status of test is FAIL.

If the De-Emphasis for a particular Preset number is not within ± 1dB of the matching value in Table 12, the status of test is FAIL.

If Swing < 2.5 dB or Swing > 4.5 dB, the status of test is FAIL.

Test References

See

- Universal Serial Bus 4 (USB Type-C) Specification Version 1.00 (Table 3-5)
- Universal Serial Bus 4 (USB Type-C) Specification Version 1.00 (Table 5-5)

Tx Electrical Idle Voltage Test

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Electrical Idle Voltage Test is to confirm that the transmitter peak voltage during electrical idle do not exceed the limits of the specification.

Test Pass Requirement

Tx Electrical Idle Voltage ≤ 20 mV_{p-p}

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 130 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group **Tx Electrical Idle Voltage** are selected.

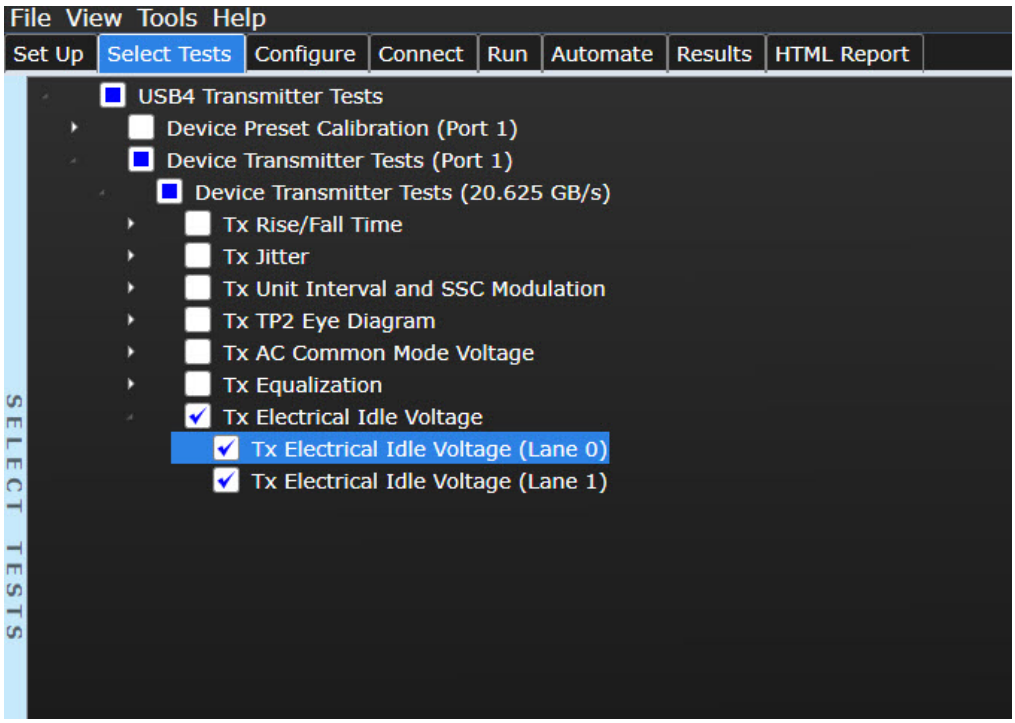


Figure 160 Selecting the Tx Electrical Idle Voltage Tests

Test Procedure

1 Configure the DUT to be in electrical idle mode.
2 Capture the waveform, and process it with the Digital Oscilloscope.
   a Sampling Rate ≥ 80 GSa/s.
   b Evaluate 10 Mpts per channel when using 80 GSa/s. For higher sampling rate, use memory depth in the same ratio to 10 Mpts.
   c No CDR, no average, and no interpolation to be used.
   d Oscilloscope must have a minimum bandwidth of 16 GHz (Gen 2) 21 GHz (Gen 3).
3 Calculate the TX Electrical Idle Voltage ($V_{\_ELEC\_IDLE}$) using this equation:
   $V_{PEAK} = V_{TX-P} - V_{TX-N}$
4 $V_{\_ELEC\_IDLE}$ shall be extracted after applying first order low-pass filter with 3 dB point at 1.25 GHz.
5 Repeat the test for the remaining USB4 lanes.

Measurement Procedure

1 Verify the input signal.
   a Verify the input signal's amplitude.
   b Scale the vertical display of the input signal to optimum value.
2 Capture the input signal, and create the differential signal.
3 Setup the parameter of the general measurement.
   a Enable measure all edges to obtain the statistical values of the measurement.
4 Setup the following measurement:
   a Peak-to-peak voltage (V_{pp})
   b Root-mean-square voltage (V_{rms})
5 Report the Electrical Idle Output Voltage measurement results.

Expected / Observable Results

$V_{\_ELEC\_IDLE}$ > 20 mV_{p-p}, the status of test is FAIL

Test References

See

- *Universal Serial Bus 4 (USB Type-C) Specification Version 1.00 (Table 3-3)*

Tx Differential Return Loss Test

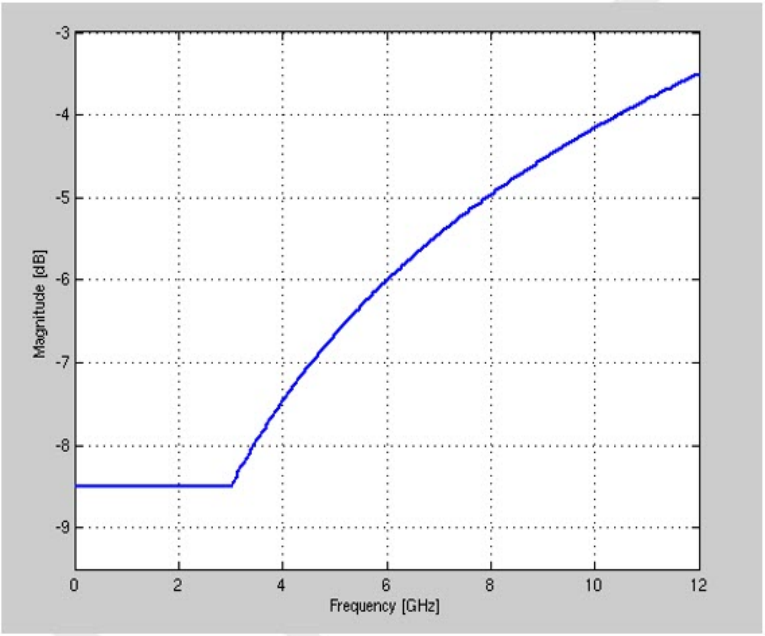
NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of this test is to confirm that the Differential Return Loss of a USB4 device is less than the maximum limit.

Test Pass Requirement

$$\mathrm{SDD11(f)} = \begin{cases} -8.5 & 0.05 < f_{GHz} \leq 3 \\ -3.5 + 8.3 \cdot \log 10\left(\frac{f_{GHz}}{12}\right) & 3 < f_{GHz} \leq 12 \end{cases}$$



Test Setup

1 For the physical connections between the DUT & the Oscilloscope, see the connection diagrams in Figure 161 and Figure 162.

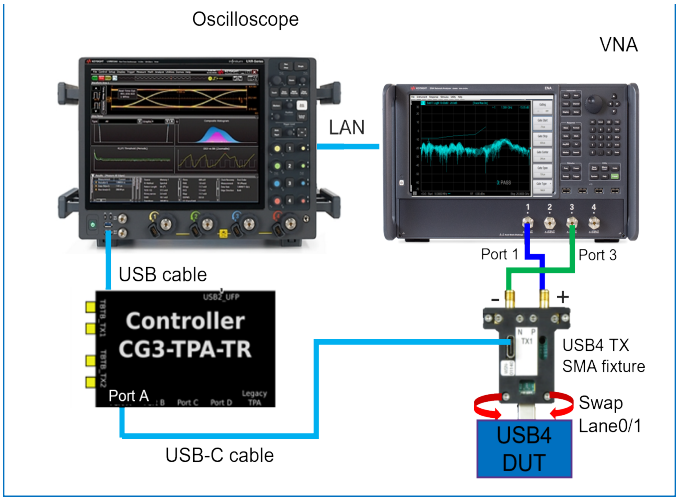


Figure 161 Tx Return loss test setup with Tx SMA test fixture

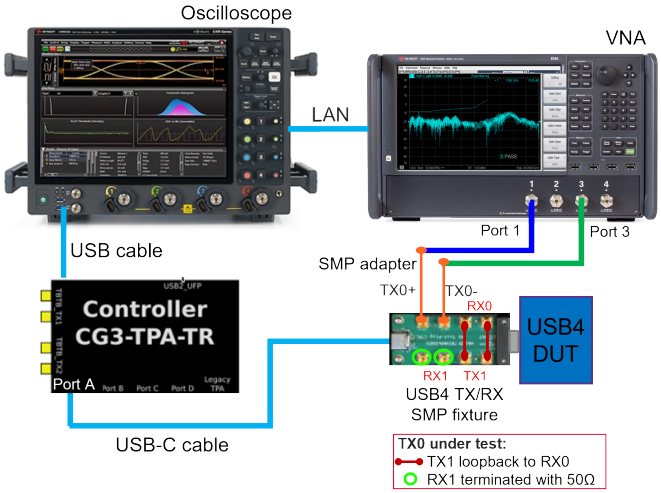
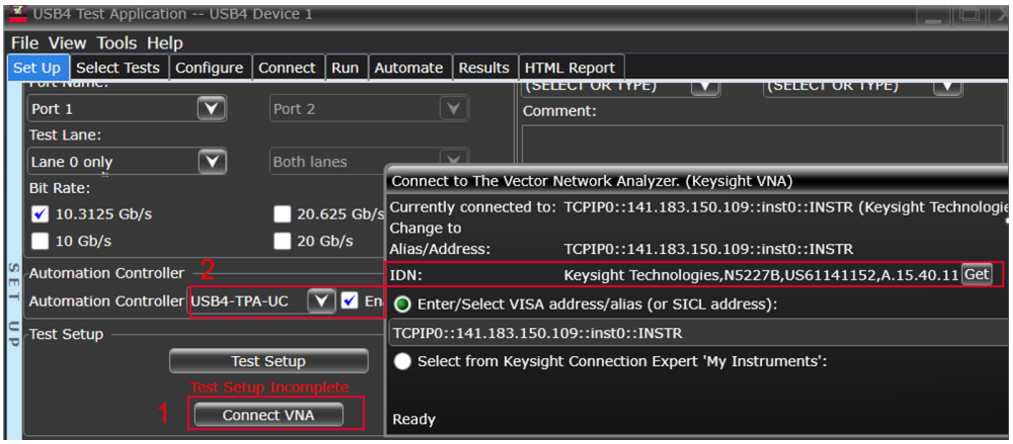


Figure 162 Return loss test setup with Tx/Rx SMP test fixture

2 In the **Set Up** tab, please connect VNA in the Tx app.

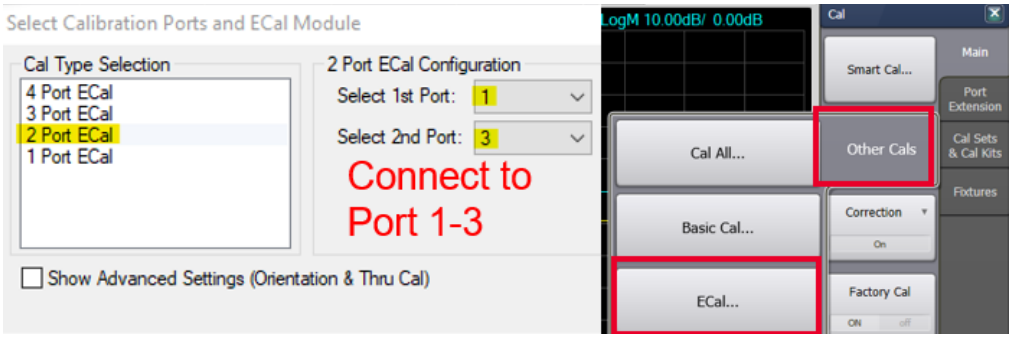


3 Prior calibration, setup Network Analyzer with following sweep settings:

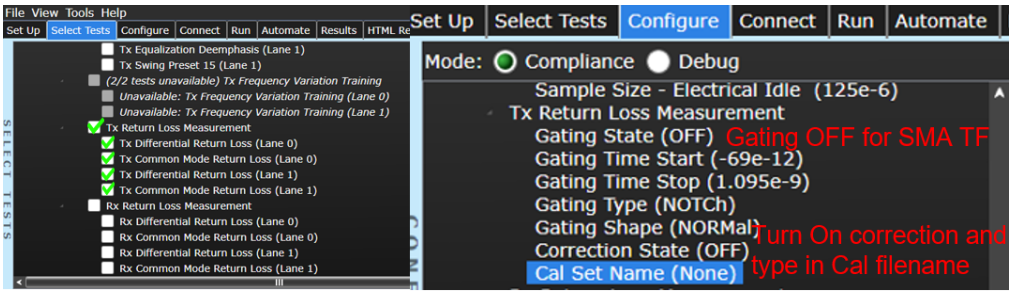
- Frequency range of 10 MHz to 12 GHz
- IF BW of 1 kHz
- At least 1600 points
- Impedance 85 ohm differential
- Define the Topology to Bal using VNA Port 1 and Port 3

NOTE Ensure that the VNA firmware revision is A.17.25.05 or higher to be compatible with the return loss test automation.

4 Run calibration on the network analyzer and test cables using a 2-port electronic kit (ECal). Save the Cal file.



5 In the **Select** test tab, select the Tx Return Loss Measurement and set the parameters in the **Configure** tab as shown in the figure below.



NOTE Please note that no gating setup is required for SMA fixture.

6 The test application sets USB4ETT **Tool Usage Mode**, commands VNA to measure Tx Return Loss in S2P, and compiles result using SigTest.

7 In the test setup, please flip the Tx fixture to swap the test lanes 0 and 1.

8 In case of SMP test fixture, Tx/Rx lane under test can be switched as shown in Figure 163.

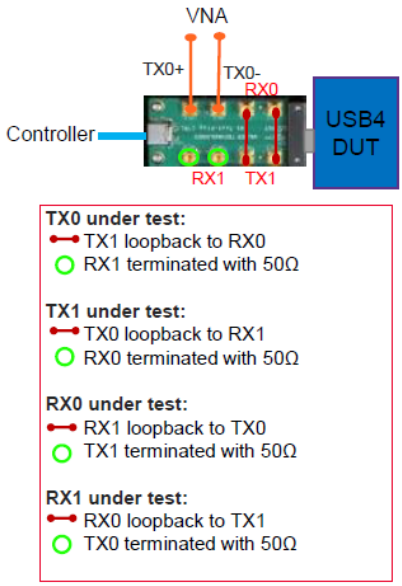


Figure 163 SMP test fixture - Tx/Rx lane switching

Test Procedure

1 Choose a supported USB4 speed to start with.
2 The test application sets USB4ETT tool to configure the DUT transmitter to output PRBS31 on all lanes with SSC turned on.
3 Connect Lane under test TX_P, TX_N to the Network Analyzer.
4 Measure the Differential R. Loss with the Network Analyzer and compile the result using SigTest.
5 If Differential Return loss violates the above requirement, then the result is Fail.
6 Repeat the test for all remaining USB4 lanes.
7 Repeat the test for all supported USB4 Gen2 and Gen3 speeds.

Expected / Observable Results

If Differential Return Loss violated the specified requirement, then Fail.

Test References

See

- *USB4 Specification Version 2.00, Table 3-2*

Tx Common Mode Return Loss Test

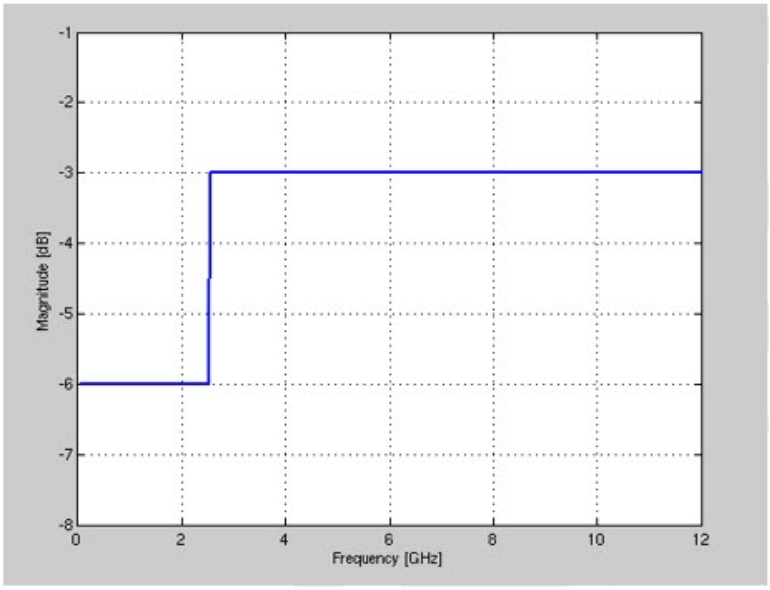
NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of this test is to confirm that the Common Mode Return Loss of a USB4 device is less than the maximum limit.

Test Pass Requirement

$$SCC11(f) = \begin{cases} -6 & 0.05 < f_{GHz} \leq 2.5 \\ -3 & 2.5 < f_{GHz} \leq 12 \end{cases}$$



Test Setup

1 For the physical connections between the DUT & the Oscilloscope, see the connection diagrams in Figure 164 and Figure 165.

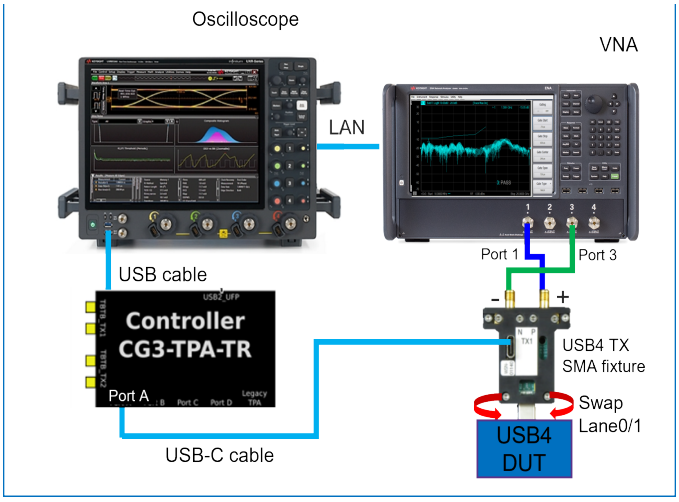


Figure 164 Tx Return loss test setup with Tx SMA test fixture

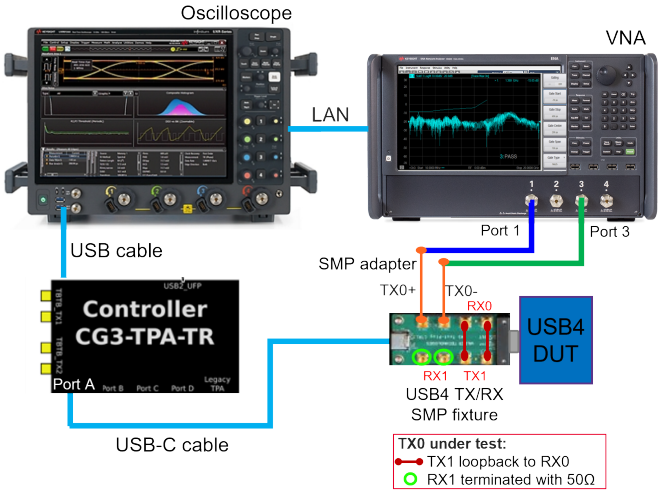
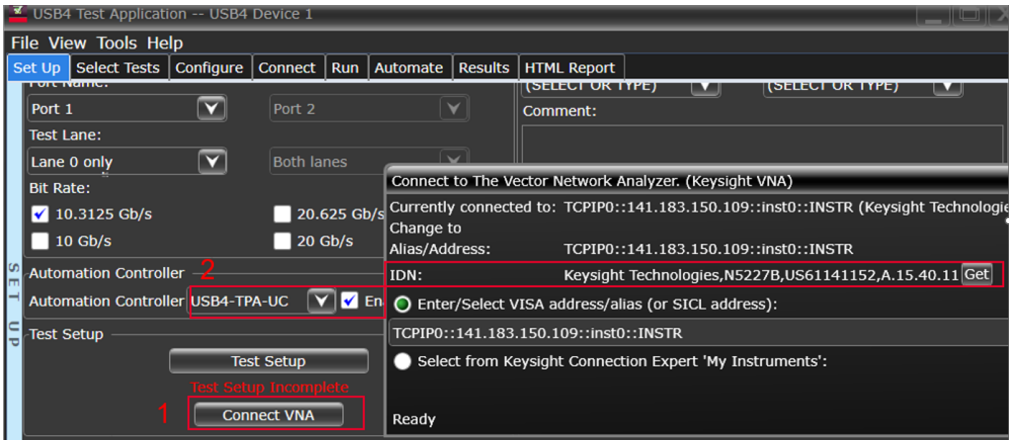


Figure 165 Return loss test setup with Tx/Rx SMP test fixture

2 In the **Set Up** tab, please connect VNA in the Tx app.

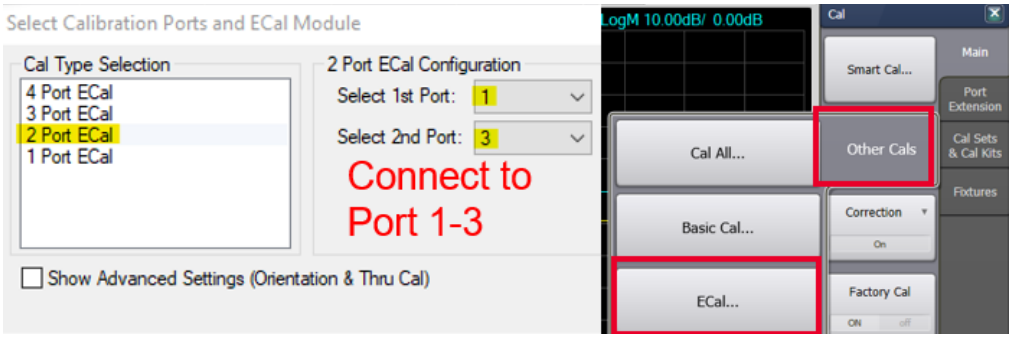


3 Prior calibration, setup Network Analyzer with following sweep settings:

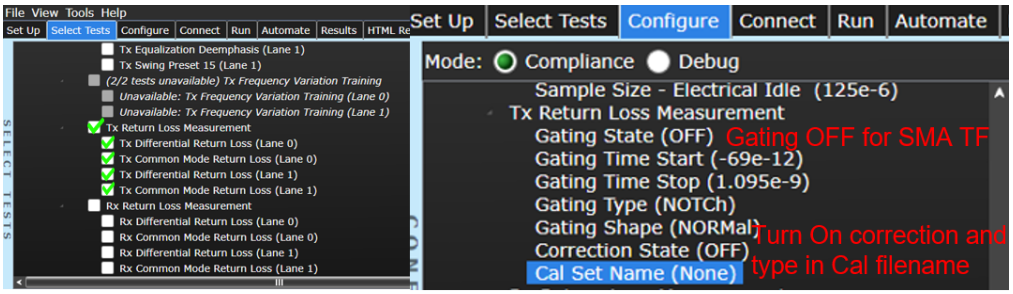
- Frequency range of 10 MHz to 12 GHz
- IF BW of 1 kHz
- At least 1600 points
- Impedance 85 ohm differential
- Define the Topology to Bal using VNA Port 1 and Port 3

NOTE Ensure that the VNA firmware revision is A.17.25.05 or higher to be compatible with the return loss test automation.

4 Run calibration on the network analyzer and test cables using a 2-port electronic kit (ECal). Save the Cal file.



5 In the **Select** test tab, select the Tx Return Loss test and set the parameters in the **Configure** tab as shown in the figure below.



NOTE Please note that no gating setup is required for SMA fixture.

6 The test application sets USB4ETT **Tool Usage Mode**, commands VNA to measure Tx Return Loss in S2P, and compiles result using SigTest.

7 In the test setup, please flip the Tx fixture to swap the test lanes 0 and 1.

8 In case of SMP test fixture, Tx/Rx lane under test can be switched as shown in Figure 166.

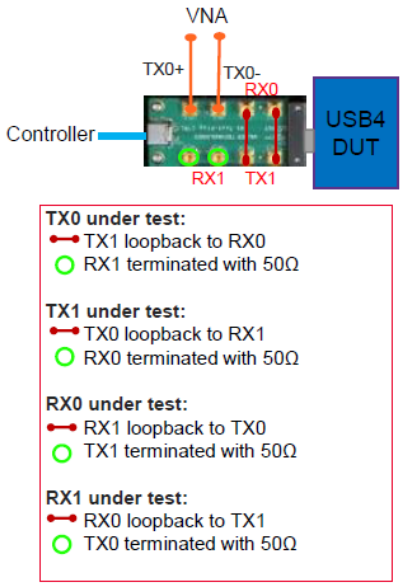


Figure 166 SMP test fixture - Tx/Rx lane switching

Test Procedure

1. Choose a supported USB4 speed to start with.
2. The test application sets USB4ETT tool to configure the DUT transmitter to output PRBS31 on all lanes with SSC turned on.
3. Connect Lane under test TX_P, TX_N to the Network Analyzer.
4. Measure the Common Mode Return Loss with the Network Analyzer and compile the result using SigTest.
5. If Common Mode Return loss violates the above requirement, then the result is Fail.
6. Repeat the test for all remaining USB4 lanes.
7. Repeat the test for all supported USB4 Gen2 and Gen3 speeds.

Expected / Observable Results

If Common Mode Return Loss violated the specified requirement, then Fail.

Test References

See

- *USB4 Specification Version 2.00, Table 3-2*

Rx Differential Return Loss Test

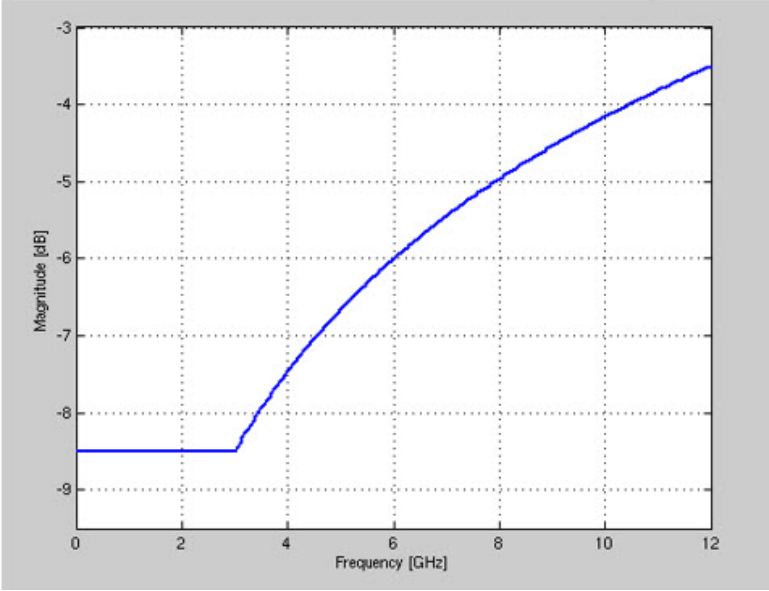
NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of this test is to confirm that the Differential Return Loss of a USB4 device is less than the maximum limit.

Test Pass Requirement

$$\mathrm{SDD22(f)} = \begin{cases} -8.5 & 0.05 < f_{GHz} \leq 3 \\ -3.5 + 8.3 \cdot \log 10\left(\frac{f_{GHz}}{12}\right) & 3 < f_{GHz} \leq 12 \end{cases}$$



Test Setup

1 For the physical connections between the DUT & the Oscilloscope, see the connection diagrams in Figure 167 and Figure 168.

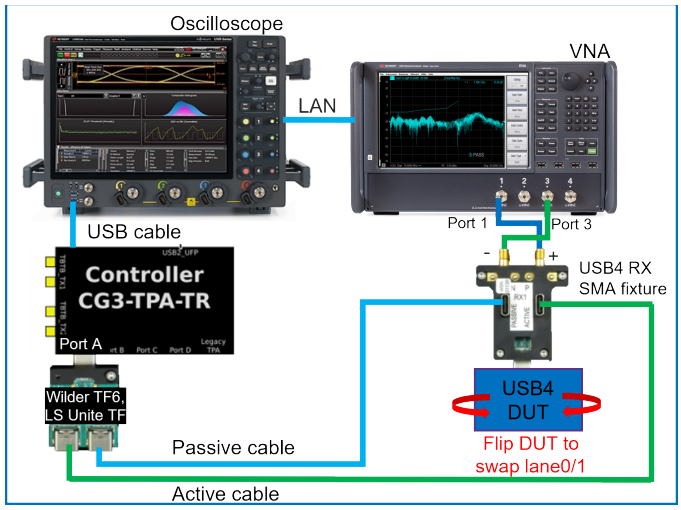


Figure 167 Tx Return loss test setup with Rx SMA test fixture

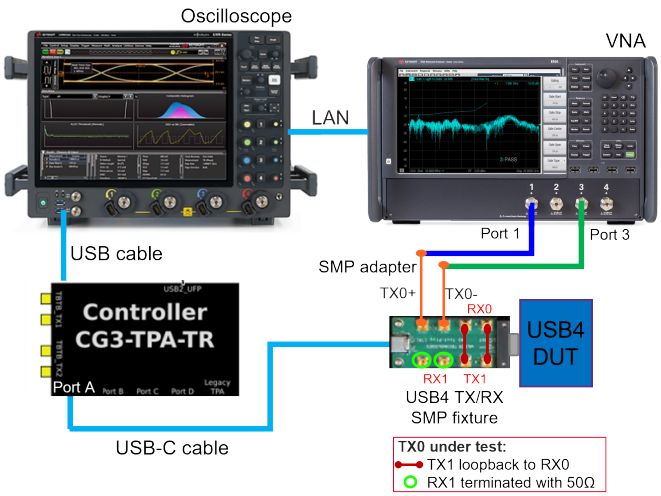
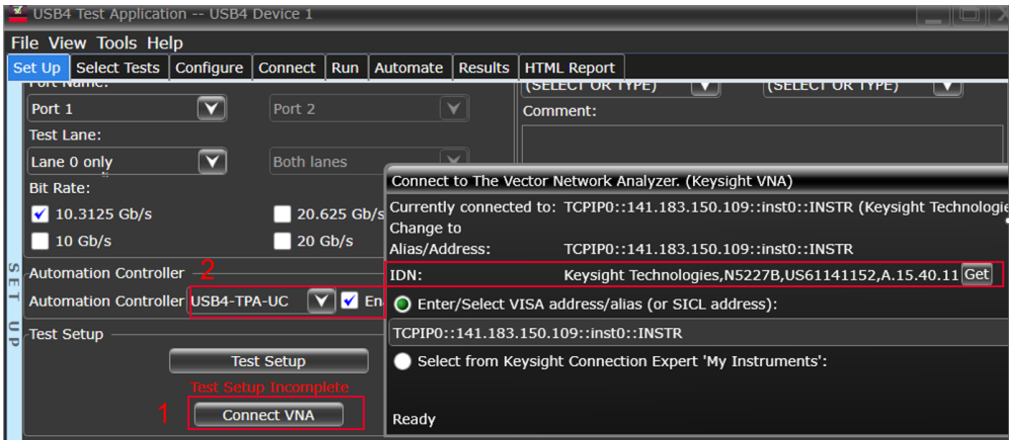


Figure 168 Return loss test setup with Tx/Rx SMP test fixture

2 In the **Set Up** tab, please connect VNA in the Tx app.

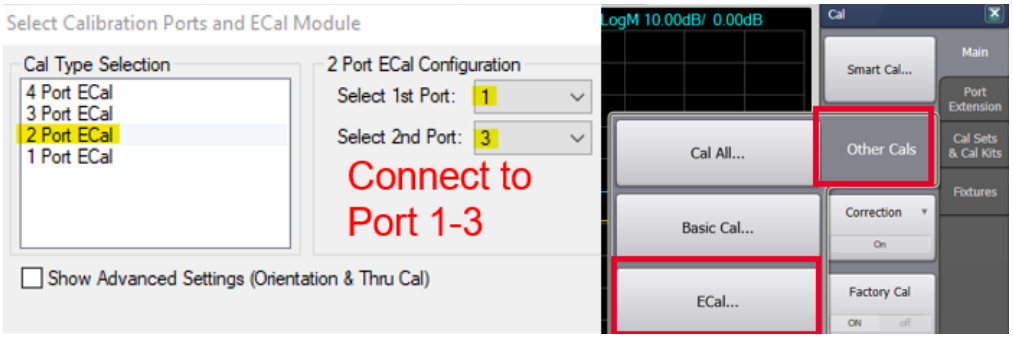


3 Prior calibration, setup Network Analyzer with following sweep settings:

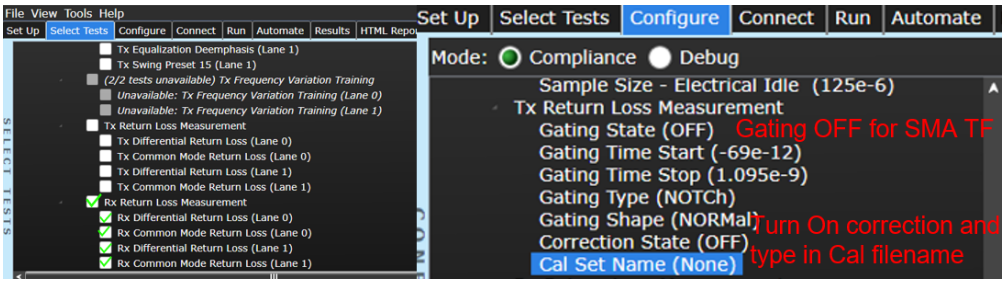
- Frequency range of 10 MHz to 12 GHz
- IF BW of 1 kHz
- At least 1600 points
- Impedance 85 ohm differential
- Define the Topology to Bal using VNA Port 1 and Port 3

NOTE Ensure that the VNA firmware revision is A.17.25.05 or higher to be compatible with the return loss test automation.

4 Run calibration on the network analyzer and test cables using a 2-port electronic kit (ECal). Save the Cal file.



5 In the **Select** test tab, select the Tx Return Loss test and set the parameters in the **Configure** tab as shown in the figure below.



NOTE Please note that no gating setup is required for SMA fixture.

6 The test application sets USB4ETT **Tool Usage Mode,** commands VNA to measure Tx Return Loss in S2P, and compiles result using SigTest.

7 In the test setup, please flip the Rx fixture to swap the test lanes 0 and 1.

8 In case of SMP test fixture, Tx/Rx lane under test can be switched as shown in Figure 169.

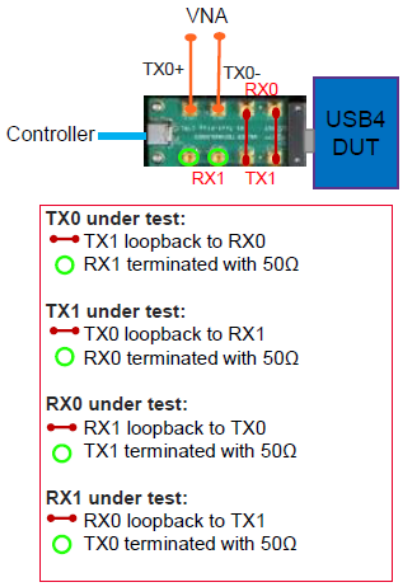


Figure 169 SMP test fixture - Tx/Rx lane switching

Test Procedure

1 Choose a supported USB4 speed to start with.
2 The test application sets USB4ETT tool to configure the DUT transmitter to output PRBS31 on all lanes with SSC turned on.
3 Connect a USB Type-C Passive cable from the Passive receptacle connector over the test fixture to the Low speed united coupon Passive receptacle connector that is connected to the USB4 Micro-controller PA.
4 Connect a USB Type-C Active cable from the Active receptacle connector over the test fixture to the Low speed united coupon Active receptacle connector that is connected to the USB4 Micro-controller PA.
5 Connect Lane under test RX_P, RX_N to the Network Analyzer.
6 Measure the Differential R. Loss with the Network Analyzer and compile the result using SigTest.
7 If Differential Return loss violates the above requirement, then the result is Fail.
8 Repeat the test for all remaining USB4 lanes.
9 Repeat the test for all supported USB4 Gen2 and Gen3 speeds.

Expected / Observable Results

If Differential Return Loss violated the specified requirement, then Fail.

Test References

See

- *USB4 Specification Version 2.00, Table 3-9*

Rx Common Mode Return Loss Test

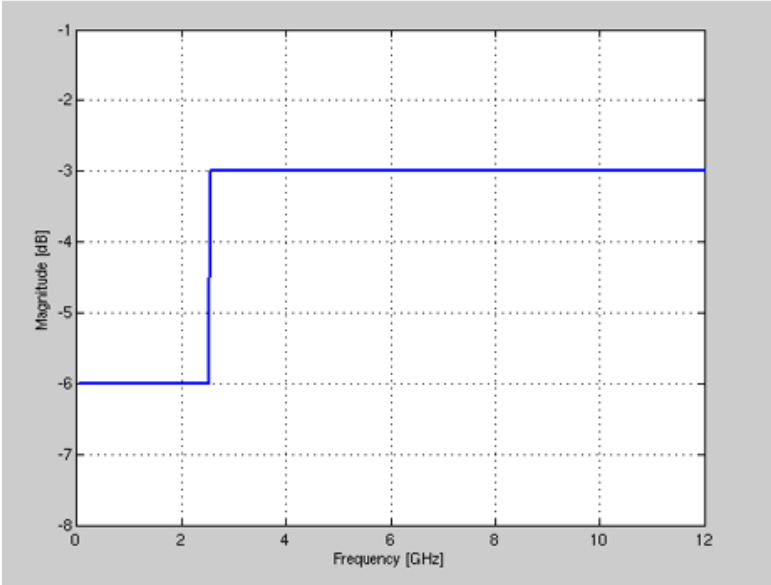
NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of this test is to confirm that the Common Mode Return Loss of a USB4 device is less than the maximum limit.

Test Pass Requirement

$$SCC22(f) = \begin{cases} -6 & 0.05 < f_{GHz} \leq 2.5 \\ -3 & 2.5 < f_{GHz} \leq 12 \end{cases}$$



Test Setup

1 For the physical connections between the DUT & the Oscilloscope, see the connection diagrams in Figure 170 and Figure 171.

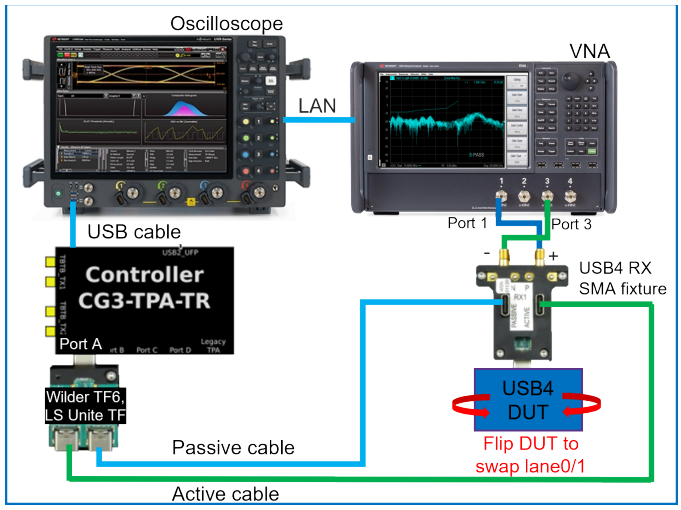


Figure 170 Tx Return loss test setup with Rx SMA test fixture

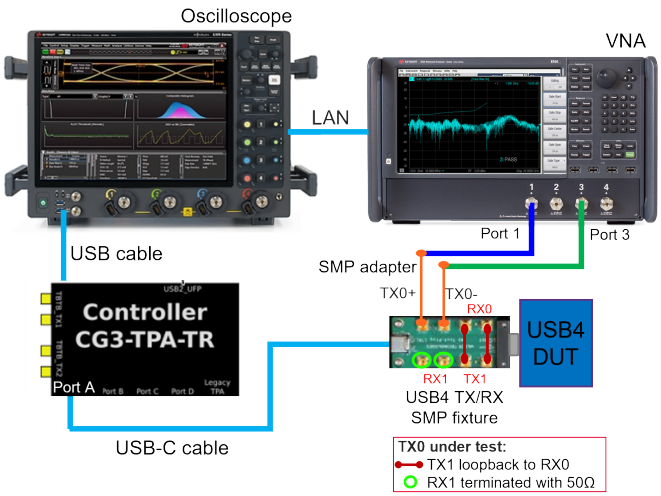
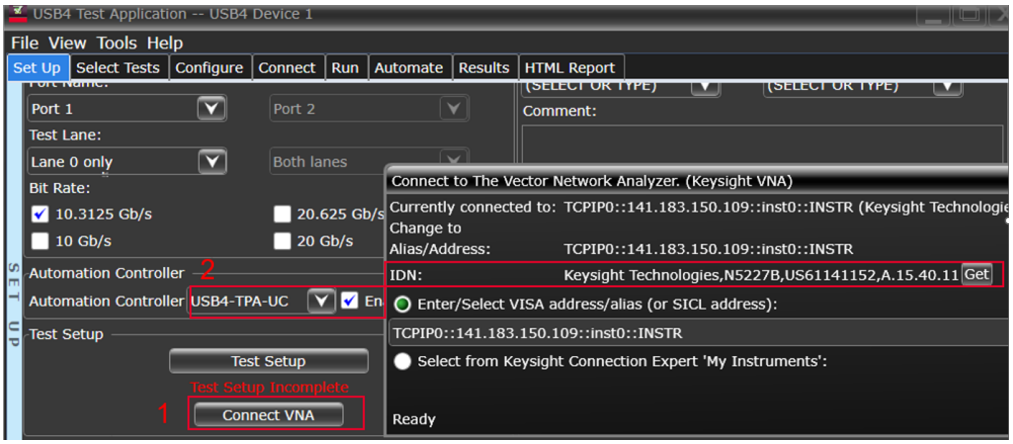


Figure 171 Return loss test setup with Tx/Rx SMP test fixture

2 In the **Set Up** tab, please connect VNA in the Tx app.

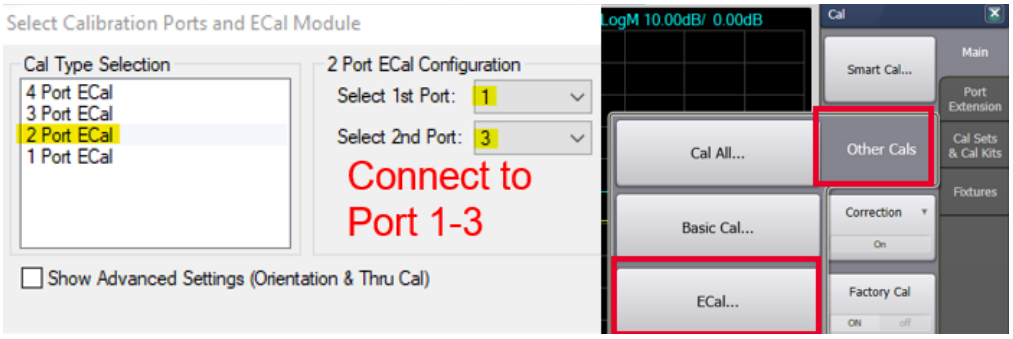


3 Prior calibration, setup Network Analyzer with following sweep settings:

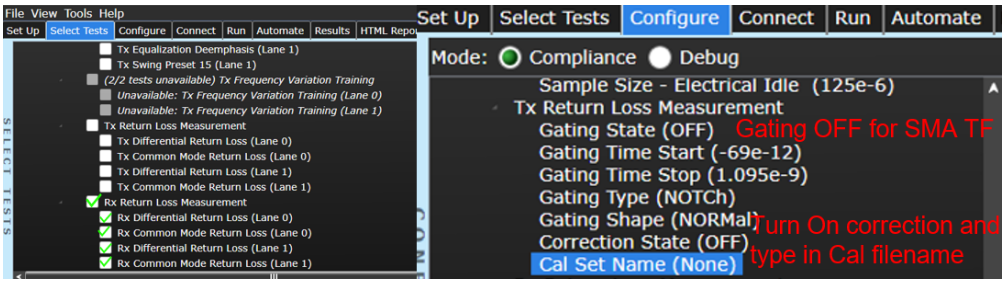
- Frequency range of 10 MHz to 12 GHz
- IF BW of 1 kHz
- At least 1600 points
- Impedance 85 ohm differential
- Define the Topology to Bal using VNA Port 1 and Port 3

NOTE Ensure that the VNA firmware revision is A.17.25.05 or higher to be compatible with the return loss test automation.

4 Run calibration on the network analyzer and test cables using a 2-port electronic kit (ECal). Save the Cal file.



5 In the **Select** test tab, select the Tx Return Loss test and set the parameters in the **Configure** tab as shown in the figure below.



NOTE Please note that no gating setup is required for SMA fixture.

6 The test application sets USB4ETT **Tool Usage Mode,** commands VNA to measure Tx Return Loss in S2P, and compiles result using SigTest.

7 In the test setup, please flip the Rx fixture to swap the test lanes 0 and 1.

8 In case of SMP test fixture, Tx/Rx lane under test can be switched as shown in Figure 172.

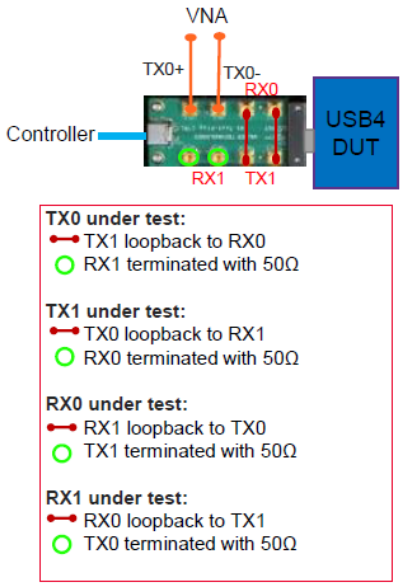


Figure 172 SMP test fixture - Tx/Rx lane switching

Test Procedure

1 Choose a supported USB4 speed to start with.
2 The test application sets USB4ETT tool to configure the DUT transmitter to output PRBS31 on all lanes with SSC turned on.
3 Connect a USB Type-C Passive cable from the Passive receptacle connector over the test fixture to the Low speed united coupon Passive receptacle connector that is connected to the USB4 Micro-controller.
4 Connect a USB Type-C Active cable from the Active receptacle connector over the test fixture to the Low speed united coupon Active receptacle connector that is connected to the USB4 Micro-controller.
5 Connect Lane under test RX_P, RX_N to the Network Analyzer.
6 Measure the Common Mode Return Loss with the Network Analyzer and compile the result using SigTest.
7 If Common Mode Return loss violates the above requirement, then the result is Fail.
8 Repeat the test for all remaining USB4 lanes.
9 Repeat the test for all supported USB4 Gen2 and Gen3 speeds.

Expected / Observable Results

If Common Mode Return Loss violated the specified requirement, then Fail.

Test References

See

USB4 Specification Version 2.00, Table 3-9

8 Transmitter Tests for 20 GB/s Systems

Tx Preset Calibration / 347
SBTX High Voltage / 350
SBTX Low Voltage / 352
SBTX Rise/Fall Time / 354
SBTX UI Duration / 357
SBRX High Voltage Detection / 360
SBRX Low Voltage Detection / 362
Tx Rise/Fall Time / 363
Tx Uncorrelated Jitter / 365
Tx Uncorrelated Deterministic Jitter / 367
Tx Data Dependent Jitter / 369
Tx Duty Cycle Distortion / 371
Tx Low Frequency Uncorrelated Deterministic Jitter / 373
Tx Total Jitter / 375
Tx Uncorrelated Jitter TP3 / 377
Tx Uncorrelated Deterministic Jitter TP3 / 379
Tx Total Jitter TP3 / 381
Tx Eye Diagram TP3 / 384
Tx Minimum Unit Interval, Min/Max / 387
Tx SSC Down Spread Rate / 389
Tx SSC Down Spread Range / 391
Tx SSC Slew Rate / 393
Tx SSC Phase Deviation / 395
Tx Eye Diagram / 397
Tx AC Common Mode Voltage / 400
Tx Equalization Tests / 402
Tx Electrical Idle Voltage Test / 407
Tx Differential Return Loss Test / 409
Tx Common Mode Return Loss Test / 414
Rx Differential Return Loss Test / 419
Rx Common Mode Return Loss Test / 424

This section provides the Methods of Implementation (MOIs) to run electrical tests on a USB DUT operating at a bit rate of 20 GB/s using an Keysight Infiniium Oscilloscope and other accessories, along with the Keysight D9040USBC USB4 Compliance Test Application.

NOTE All USB4 devices that support a bit rate of 20 Gb/s are classified as Gen3 devices.

Tx Preset Calibration

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Preset Calibration Test is to find the optimized preset for the platform.

NOTE Prior to running the compliance tests, the Host / Device must go through Preset Calibration.

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 174 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Preset Calibration* are checked.

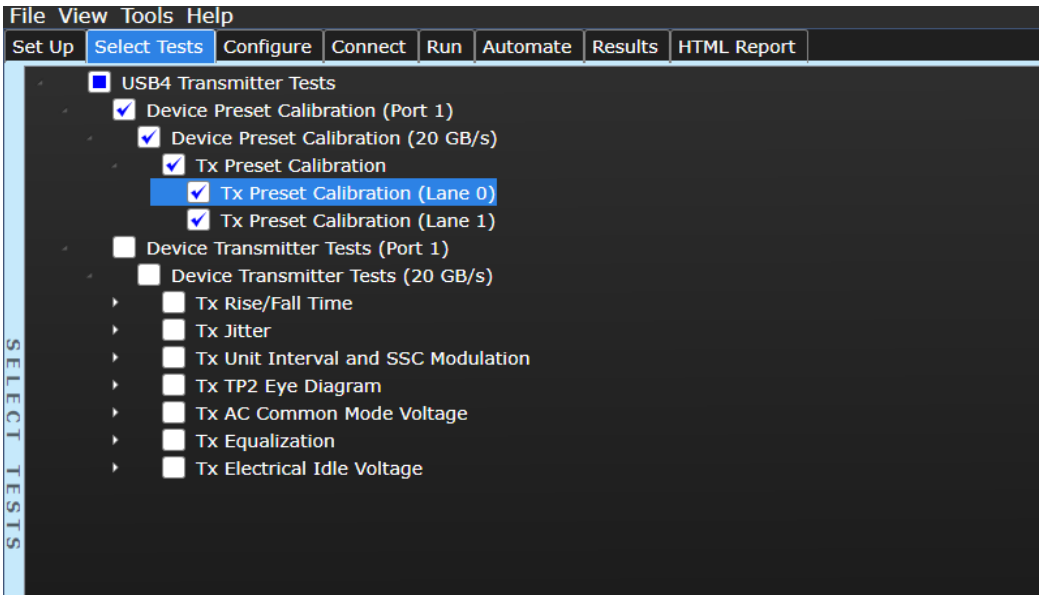


Figure 173 Selecting the Tx Preset Calibration tests

NOTE By default, the test group for **Preset Calibration** for each selected bit-rate is hidden in the **Select Tests** tab when **Predefined Optimum Preset Number** is selected for the respective bit-rates. To view and select the **Preset Calibration** tests in the **Select Tests** tab, select the **Run Preset Calibration** option in the **Test Setup** window of the **Set Up** tab.

NOTE

In the **Measurement Server** mode or **Multi** instance mode, it is recommended to run the **Tx Preset Calibration** tests first to get the optimized preset value. Then use this value to run the remaining transmitter tests.

Detailed Process:

In the **Measurement Server** mode or **Multi** instance mode, after running the **Preset Calibration** test, please see the HTML Report and note down the optimized preset value. Then, please navigate to **Set Up** tab > **Test Setup** button > **Test Setup** dialog box. Select the check box "Predefined Optimum Preset Number", use the already noted optimized preset number, and manually **Select the Optimum Preset Number for Each Bit Rate**. Now, please run the rest of the transmitter tests.

USB4 Microcontroller and Test Adapter USB Test Set-up

The figure, below, shows a simplified set-up example of a USB4 Microcontroller and a US4B Test Adapter used to test a typical USB DUT.

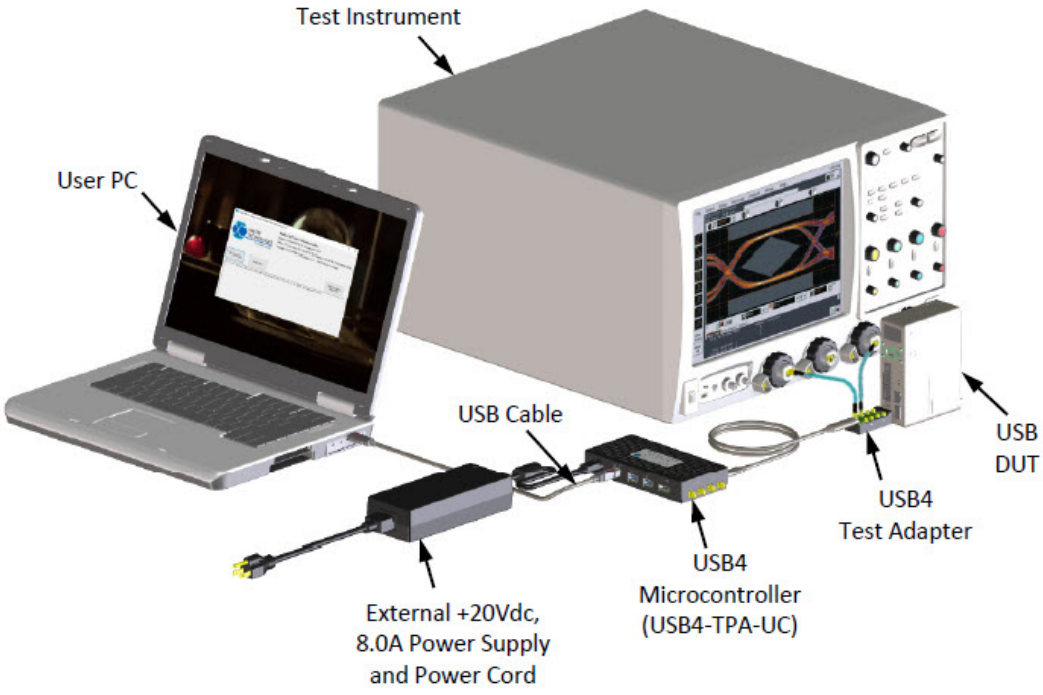


Figure 174 Transmitter TP2/TP3 Test Setup

Test Procedure

1 Connect the DUT to the Oscilloscope as shown in the Figure 174.
2 Choose a USB4 speed to start with.
3 Configure the DUT transmitter to output PRBS15, preset 0 on all lanes with SSC enabled.
4 The cables from the plug test fixture to the scope shall be de-embedded.
5 Perform measurements with:
   a Reference CDR modeled by a 2^{nd} order PLL response which drives High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used.
   b Oscilloscope with a minimum bandwidth of 21 GHz.
6 Capture the waveform and process it with the digital oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Evaluate 40 Mpts per channel when using 80 GSa/s. For higher sample rate use memory depth in the same ration to 40 Mpts.
   c Pattern length - Periodic
   d Jitter separation method shall be suitable for cross talk on signal
   e Adjust vertical scale to fit signal into scope screen.
   f Referenced to 1E-13 statistics.
7 Capture DDJ results for lane 0.
8 Repeat the test for all remaining USB4 transmit presets (till preset 15 as shown in Table 5).
9 Repeat the test for the remaining USB4 lanes.
10 For each lane, choose the preset that provides minimum DDJ.
11 Repeat the above procedure for all supported USB4 speeds.

Expected / Observable Results

For each lane, the preset that provides the minimum DDJ is the optimized preset for the platform.

Test References

See

- *Universal Serial Bus 4 (USB Type-C) Specification Version 1.00 (Table 3-5)*

SBTX High Voltage

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of this test is to confirm that the SBTX High Voltage Measurement of a USB4 device is within the specification limits.

Test Pass Requirement

2.40 V ≤ SBTX High Voltage Measurement ≤ 3.52 V

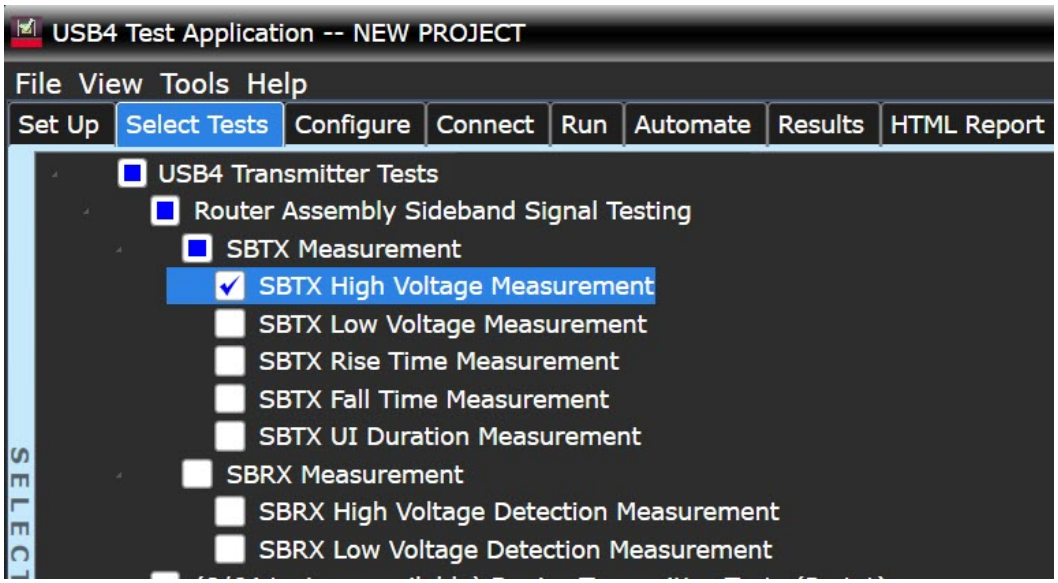
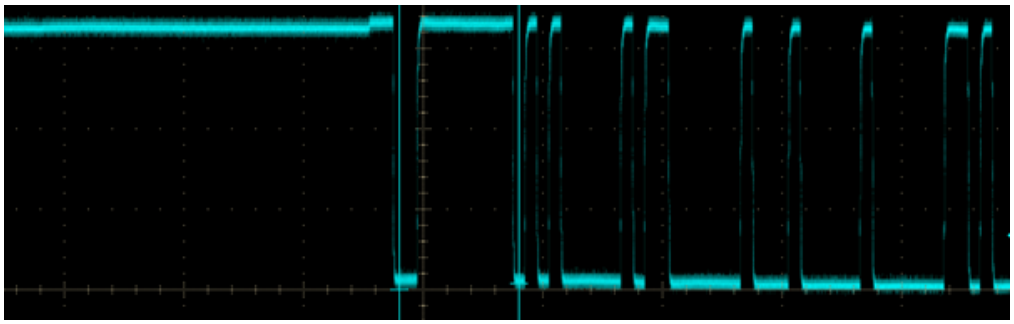


Figure 175 Selecting the SBTX High Voltage Measurement test

Test Procedure

1. Connect a voltage meter/DMMfluke to SBU1 header in the USB4 Test Fixture.
2. Power up the DUT.
3. Measure the voltage.
4. If $SBTX_{VOH}$ < 2.4 V or > 3.52 V then Fail.
5. Connect a scope with high impedance probe to the SBU1 header in the USB4 Test Fixture.
6. In the scope use a trigger based on pulse width, negative polarity, trigger when the pulse width <10 µs and threshold of 600 mV.
7. Horizontal scale = 10 µs per square, vertical scale = 1 V per square.
8. Power up the DUT.

9 Over the Infiniium Oscilloscope the trigger shall capture the transaction pattern.



10 Measure the high/low value of the "1" amplitude for a bit inside the transaction. Over/undershoot shall be ignored.

11 If $SBTX_{VOH}$ < 2.4 V or > 3.52 V then Fail.

Expected / Observable Results

If $SBTX_{VOH}$ < 2.4 V or > 3.52 V then Fail.

Test References

See

- *USB4 Specification Version 2.00 (Table 3-32)*

SBTX Low Voltage

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of this test is to confirm that the SBTX Low Voltage Measurement of a USB4 device is within the specification limits.

Test Pass Requirement

2.40 V ≤ SBTX Low Voltage Measurement ≤ 3.52 V

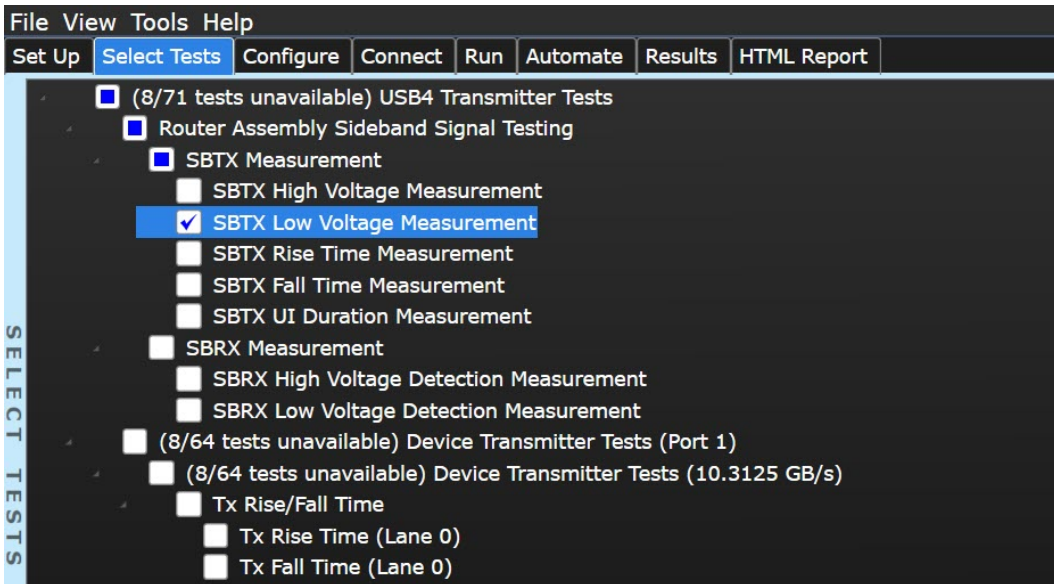


Figure 176 Selecting the SBTX Low Voltage Measurement test

Test Procedure

1. Connect a voltage meter/DMMfluke to SBU1 header in the USB4 Test Fixture.
2. DUT shall be in power down state.
3. Measure the voltage.
4. If $SBTX_{VOL}$ < -0.05 V or > 0.4 V then Fail.
5. Connect a scope with high impedance probe to the SBU1 header in the USB4 Test Fixture.
6. In the scope use a trigger based on pulse width, negative polarity, trigger when the pulse width <10 µs and threshold of 600 mV.
7. Horizontal scale = 10 µs per square, vertical scale = 1 V per square.
8. Connect link partner to the DUT.
9. Over the Infiniium Oscilloscope the trigger shall capture the transaction pattern.

10 Measure the high/low value of the "0" amplitude for a bit inside the transaction. Over/undershoot shall be ignored.

11 If $SBTX_{VOL}$ < -0.05 V or > 0.4 V then Fail.

Expected / Observable Results

If $SBTX_{VOL}$ < -0.05 V or > 0.4 V then Fail.

Test References

See

- *USB4 Specification Version 2.00 (Table 3-32)*

SBTX Rise/Fall Time

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of this test is to confirm that the SBTX Rise/Fall Time Measurement of a USB4 device is within the specification limits.

Test Pass Requirement

$3.5\ ns \leq SBX_{TRTF} \leq 65\ ns$.

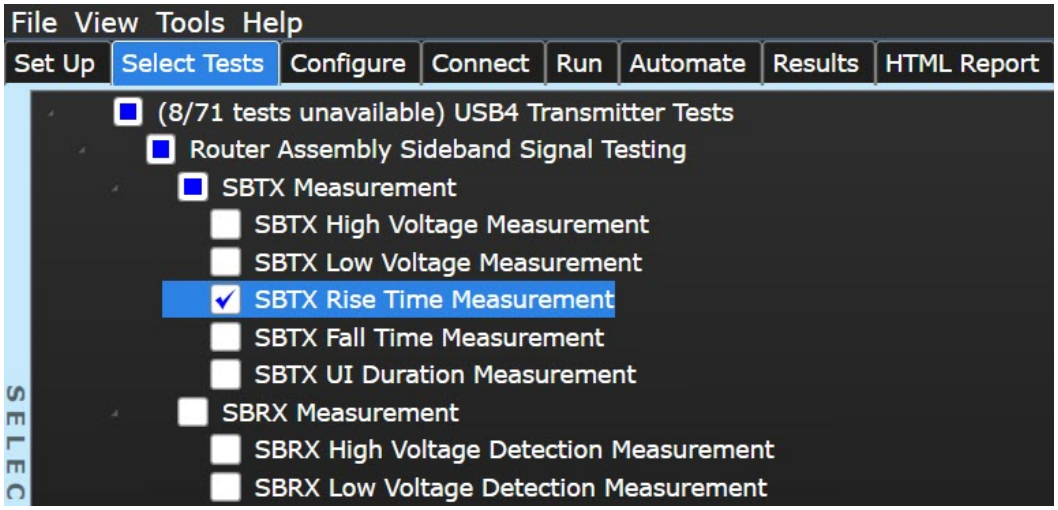


Figure 177 Selecting the SBTX Rise Time Measurement test

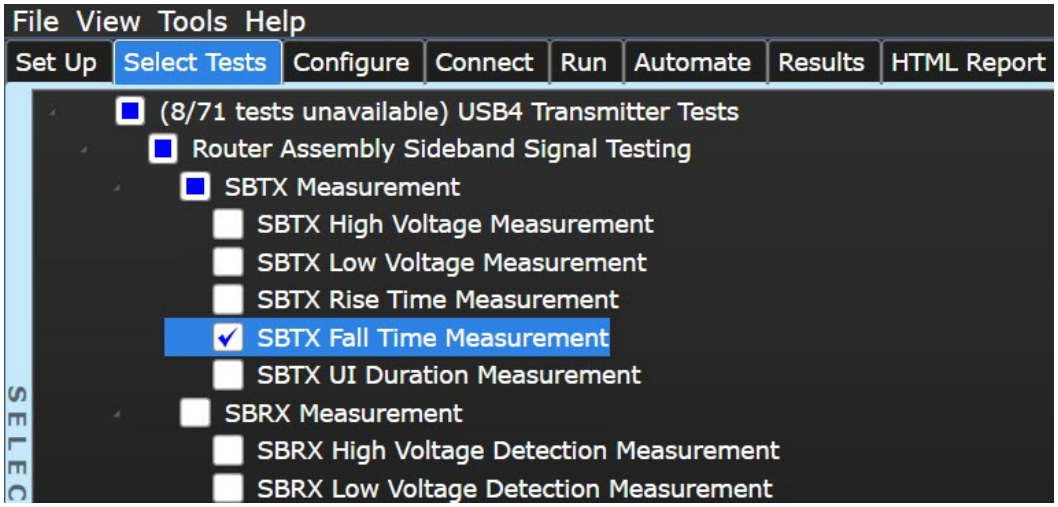
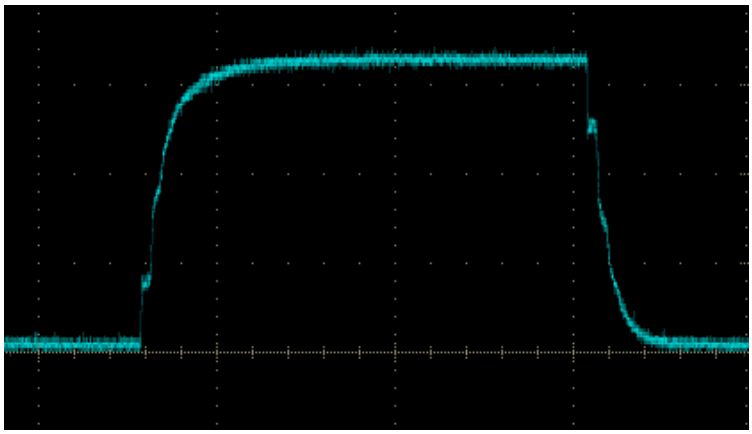


Figure 178 Selecting the SBTX Fall Time Measurement test

Test Procedure

1 Connect the DUT via USB4 Test Fixture with USB4 u-controller in order to establish link.
2 The measurement shall be in transaction only and not from power down to up (or the opposite).
3 Connect a scope with high impedance probe to the SBU1 header for SBTX test in the USB4 Test Fixture.
4 In the scope use a trigger based on pulse width, negative polarity, trigger when the pulse width <10 µs and threshold of 600 mV.
5 Horizontal scale = 10 µs per square, vertical scale = 1 V per square.
6 Power up the DUT.
7 Over the Infiniium Oscilloscope the trigger shall capture the transaction pattern.
8 Zoom in one bit from inside the transaction pattern. Not the 1st or the last bit.



9 Measure the rise and fall time (10%-90%) for SBTX.
10 If 65 ns < STX_{TRTF} < 3.5 ns then Fail.

Expected / Observable Results

If 65 ns < STX_{TRTF} < 3.5 ns then Fail.

Test References

See

- *USB4 Specification Version 2.00 (Table 3-32)*

SBTX UI Duration

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of this test is to confirm that the SBTX UI Duration Measurement of a USB4 device is within the specification limits.

Test Pass Requirement

970 ns ≤ SBX_{UI} ≤ 1030 ns.

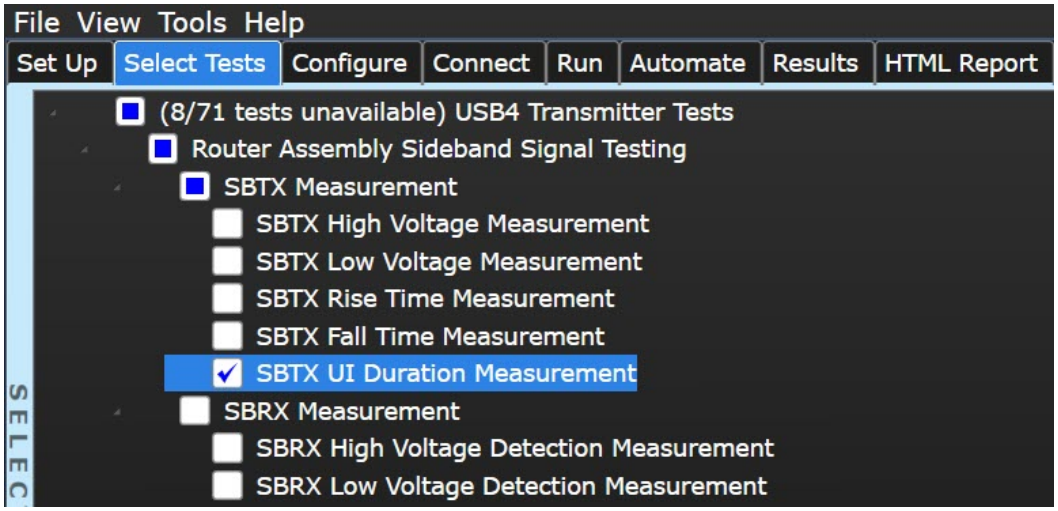
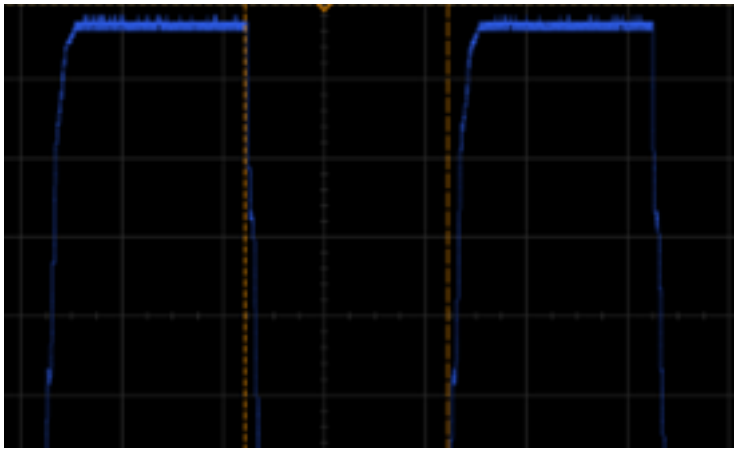


Figure 179 Selecting the SBTX UI Duration Measurement test

Test Procedure

1 Connect the DUT via USB4 Test Fixture with USB4 u-controller in order to establish link.
2 The measurement shall be in transaction only, over the transaction pattern.
3 Connect a scope with high impedance probe to the SBU1 header for SBTX test in the USB4 Test Fixture.
4 In the scope use a trigger based on pulse width, negative polarity, trigger when the pulse width <10 µs and threshold of 600 mV.
5 Horizontal scale = 10 µs per square, vertical scale = 1 V per square.
6 Power up the DUT.
7 Over the Infiniium Oscilloscope the trigger shall capture the transaction pattern.
8 Zoom in "10" bits from the transaction pattern.



9 Measure the duration from falling edge of the "1" to the rising edge of "0", named SBX_UI.
10 If 970 ns < $SBTX_{UI}$ < 1030 ns then Fail.

Expected / Observable Results

If 970 ns < $SBTX_{UI}$ < 1030 ns then Fail.

Test References

See

- *USB4 Specification Version 2.00 (Table 3-32)*

SBRX High Voltage Detection

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of this test is to confirm that the SBRX High Voltage Detection Measurement of a USB4 device is within the specification limits.

Test Pass Requirement

$2.0\ V \leq SBRX_{VIH} \leq 3.77\ V$

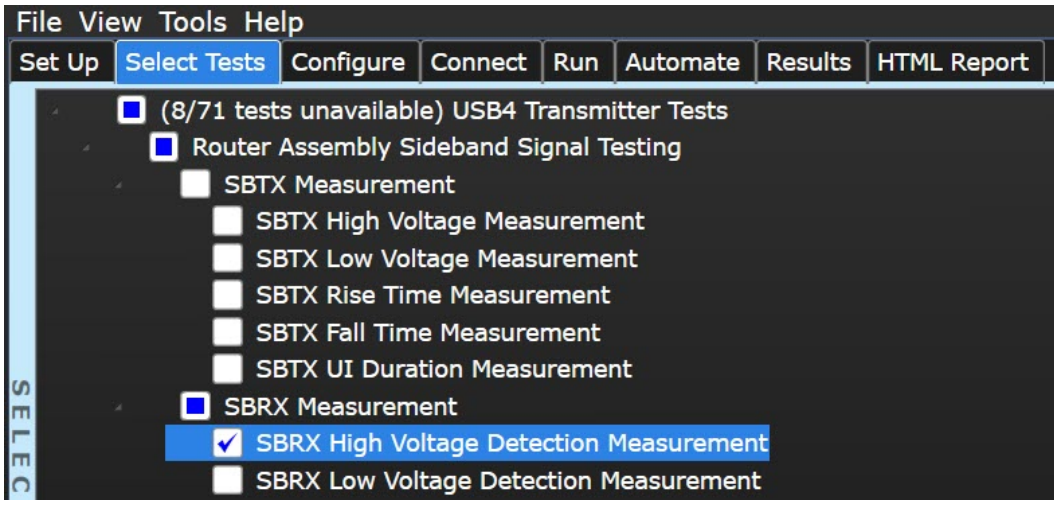
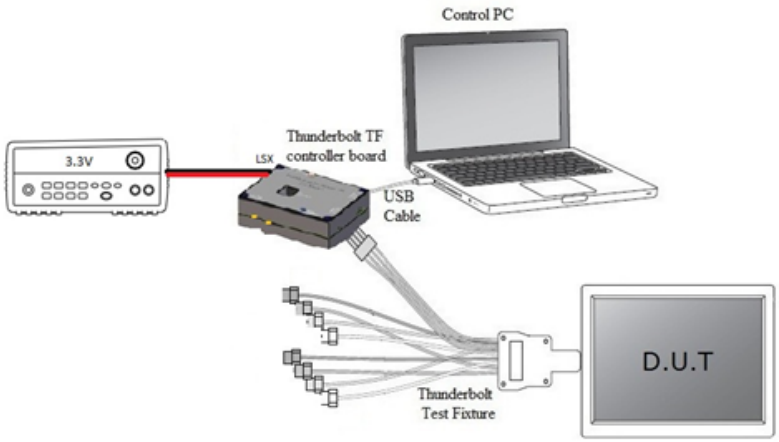


Figure 180 Selecting the SBRX High Voltage Measurement test

Test Procedure

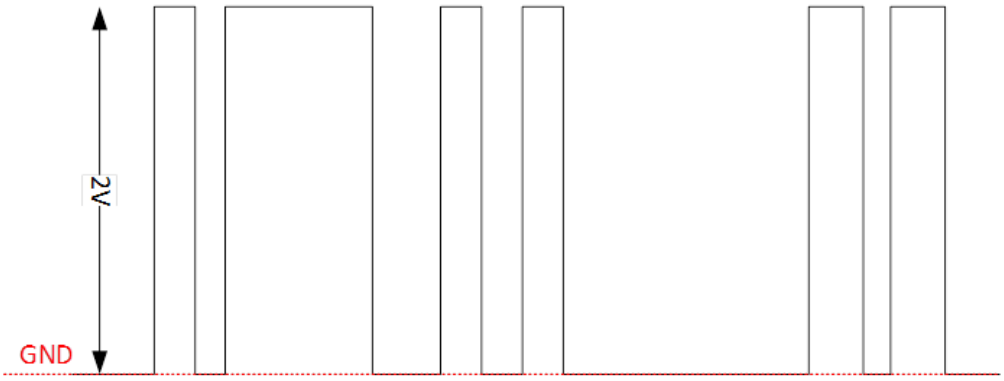
1 Connect the DUT via USB4 LSXX Test Fixture with USB4 u-controller and set '1' bit amplitude to 3.3 V and '0' bit amplitude to 0 V in order to establish link.



2 Set the 3.3 V power supply to 3.77 V.

3 Establish there is a link.

4 Reduce the external power supply to 2.0 V.



5 If link is lost, then Fail.

Expected / Observable Results

2.0 V ≤ $SBRX_{VIH}$ ≤ 3.77 V

Test References

See

- *USB4 Specification Version 2.00 (Table 3-32)*

SBRX Low Voltage Detection

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of this test is to confirm that the SBRX Low Voltage Detection Measurement of a USB4 device is within the specification limits.

Test Pass Requirement

$-0.3\ V \leq SBRX_{VIL} \leq 0.65\ V$

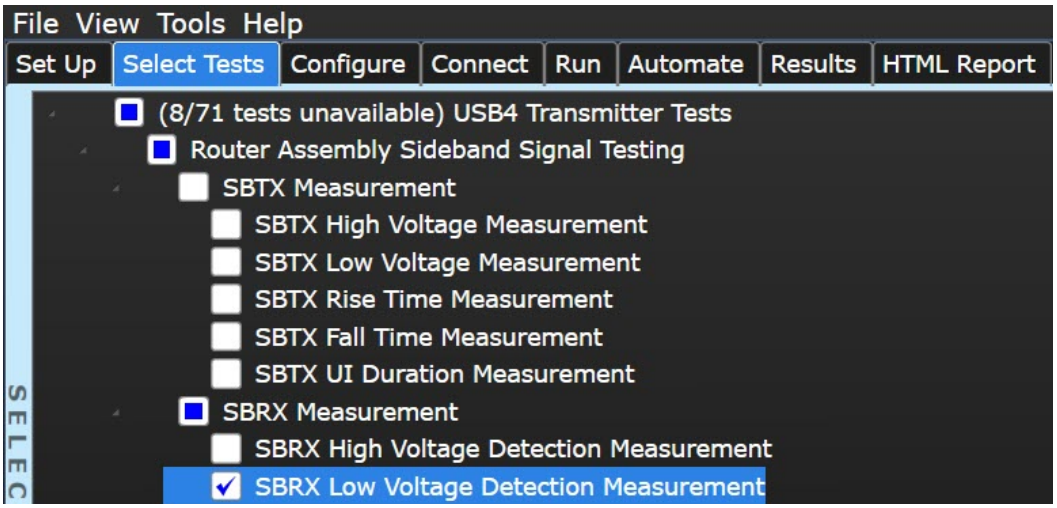


Figure 181 Selecting the SBRX Low Voltage Measurement test

Test Procedure

1. Connect the DUT via USB4 Test Fixture with USB4 u-controller with external 3.3 V power supply connected to the SBX input in order to establish link.
2. Set the 3.3 V power supply to 3.3 V.
3. Establish there is a link.
4. Reduce the external power supply to 0.65 V.
5. If link is established, then Fail.

Expected / Observable Results

$-0.3\ V \leq SBRX_{VIL} \leq 0.65\ V$

Test References

See

- *USB4 Specification Version 2.00 (Table 3-32)*

Tx Rise/Fall Time

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Rise/Fall Time Test is to confirm that the rise times and fall times on the USB differential signals are within the limits of the specification.

Test Pass Requirement

Rise Time and Fall Time $\geq$ 10 ps (Refer to Table 9 on page 86).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 174 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Rise/Fall Time* are checked.

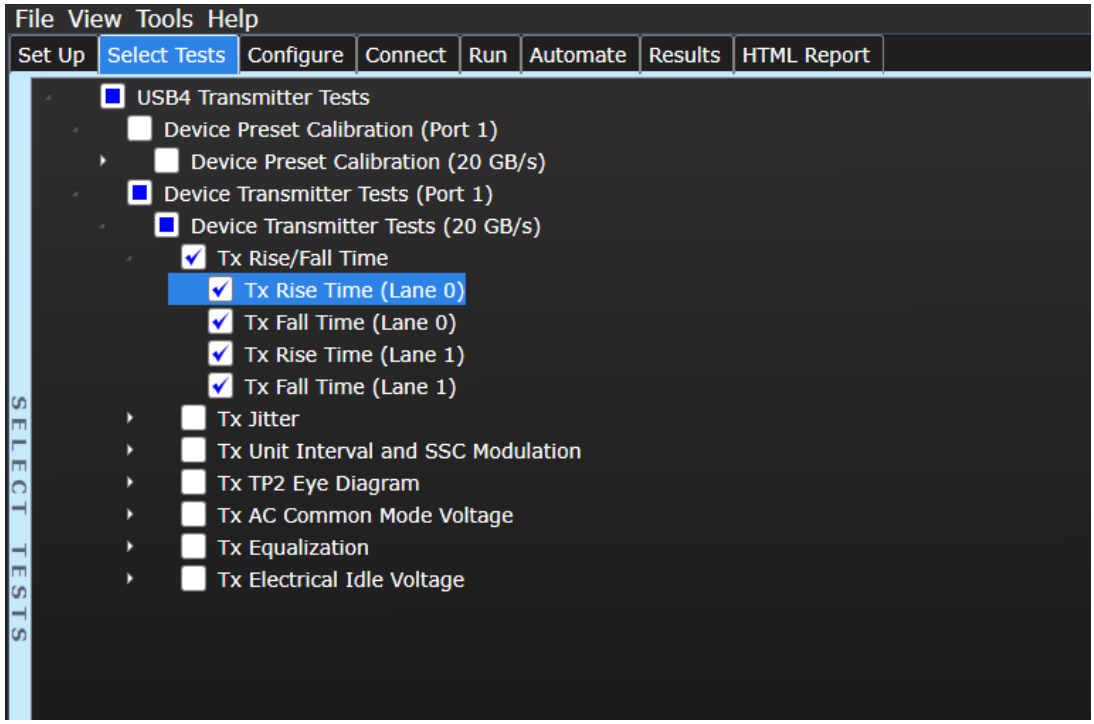


Figure 182 Selecting the Tx Rise/Fall Time tests

Test Procedure

1. Configure DUT transmitter to output alternating square pattern of 64 0's and 64 1's (SQ128) on all lanes with SSC turned on.
2. Evaluate at least 4Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ratio to 4Mpts. Use the maximum analog bandwidth of the Oscilloscope.

   No CDR, no average and no interpolation to be used.

   Adjust vertical scale such that the signal fits within the Oscilloscope's display.
3. Measure T_{RISE} as the mode of the sampled edge times from 20% to 80% of the differential swing voltage rising edge.
4. Measure T_{FALL} as the mode of the sampled edge times from 80% to 20% of the differential swing voltage falling edge.
5. Repeat the test for the remaining USB lanes.

Expected / Observable Results

If T_{RISE} < 10ps, the status of test is FAIL.

If T_{FALL} < 10ps, the status of test is FAIL.

Test References

See

- Universal Serial Bus 4 (USB Type-C) Specification Version 1.00 (Table 3-3)

Tx Uncorrelated Jitter

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Uncorrelated Jitter Test is to confirm that the Uncorrelated Jitter [Deterministic Jitter (DJ) and Random Jitter (RJ) components] of the transmitter is within the limits of the specification.

Test Pass Requirement

Uncorrelated Jitter (UJ) $\leq$ 0.31 UI_{p-p} (Refer to Table 8 on page 85).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 174 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter, Data Dependent Jitter and Duty Cycle Distortion* are checked.

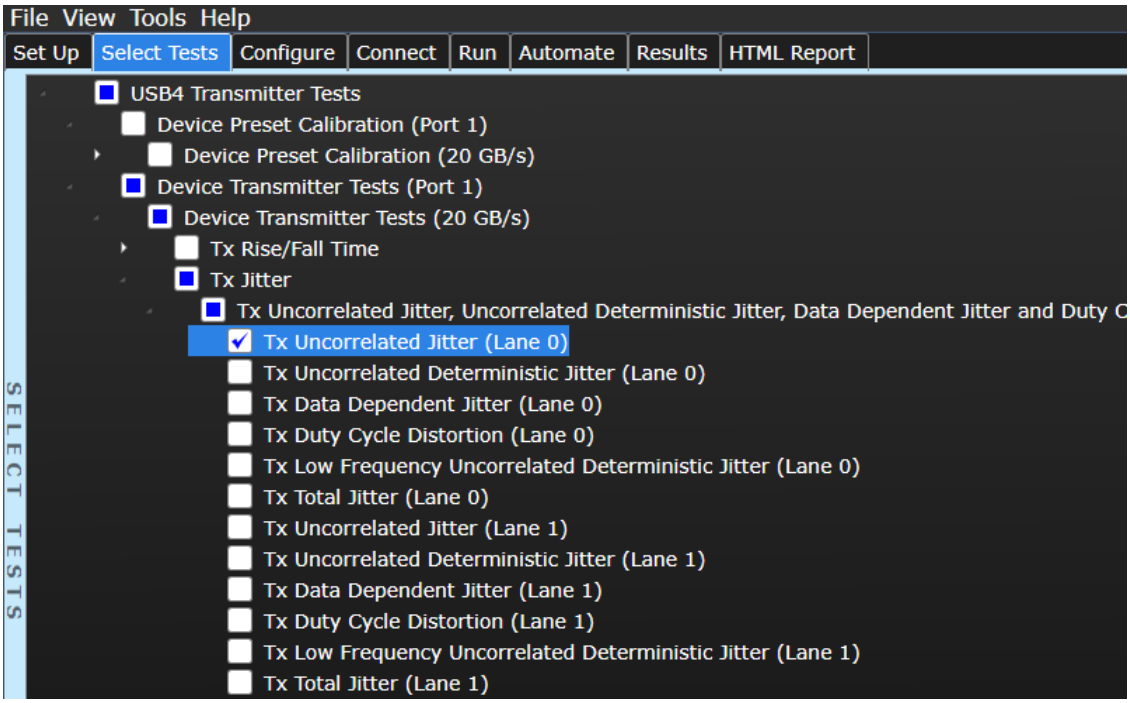


Figure 183 Selecting the Tx Uncorrelated Jitter tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2 Perform measurements with:
   a Reference CDR based on the 2^{nd} order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   b Oscilloscope with a bandwidth of 21GHz
3 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Pattern length – Periodic
   c Jitter Separatio method must be suitable for cross-talk on the signal
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Evaluate 40 Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ratio to 40 Mpts
   f Referenced to 1E-13 statistics
4 Capture the Total Jitter (TJ) and Data Dependent Jitter (DDJ) results.
5 Calculate UJ using the equation:

$$UJ = TJ - DDJ$$

6 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If UJ > 0.31 UI_{p-p}, the status of test is FAIL.

Test References

See

- *Universal Serial Bus 4 (USB Type-C) Specification Version 1.00 (Table 3-8)*

Tx Uncorrelated Deterministic Jitter

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Uncorrelated Deterministic Jitter Test is to confirm that the Uncorrelated Deterministic Jitter of the transmitter is within the limits of the specification.

Test Pass Requirement

Uncorrelated Deterministic Jitter (UDJ) $\leq$ 0.17 UI_{p-p} (Refer to Table 8 on page 85).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 174 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter, Data Dependent Jitter and Duty Cycle Distortion* are checked.

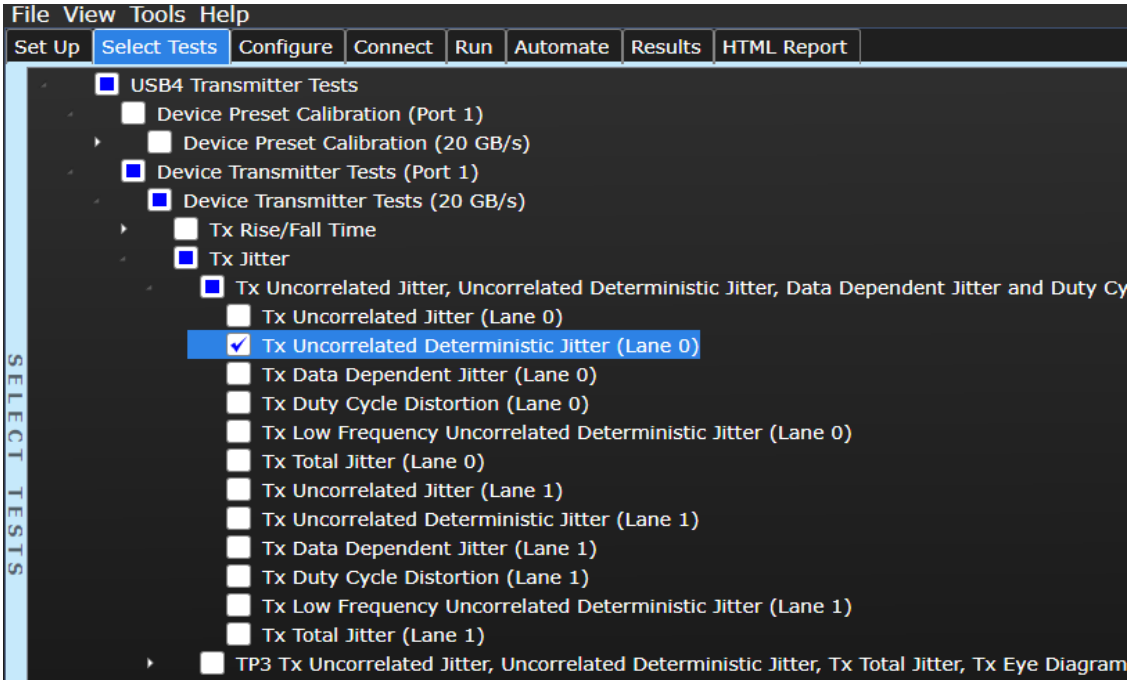


Figure 184 Selecting the Tx Uncorrelated Deterministic Jitter tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2 Perform measurements with:
   a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   b Oscilloscope with a bandwidth of 21GHz
3 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Pattern length – Periodic
   c Jitter Separation method must be suitable for cross-talk on the signal
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Evaluate 40 Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ratio to 40 Mpts
   f Referenced to 1E-13 statistics
4 Capture the UDJ result (same as BUJ over the Oscilloscope).
5 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If UDJ > 0.17 UI_{p-p}, the status of test is FAIL.

Test References

See

- *Universal Serial Bus 4 (USB Type-C) Specification Version 1.00 (Table 3-8)*

Tx Data Dependent Jitter

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Data Dependent Jitter Test is to confirm that the sum of Data Dependent Jitter (DDJ) of a USB4 device must be less than the maximum limit as per the specification.

Test Pass Requirement

Data Dependent Jitter (DDJ) $\leq$ 0.21 UI_{p-p} (Refer to Table 8 on page 85).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 174 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the tests under the test group *Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter, Data Dependent Jitter and Duty Cycle Distortion* are selected.

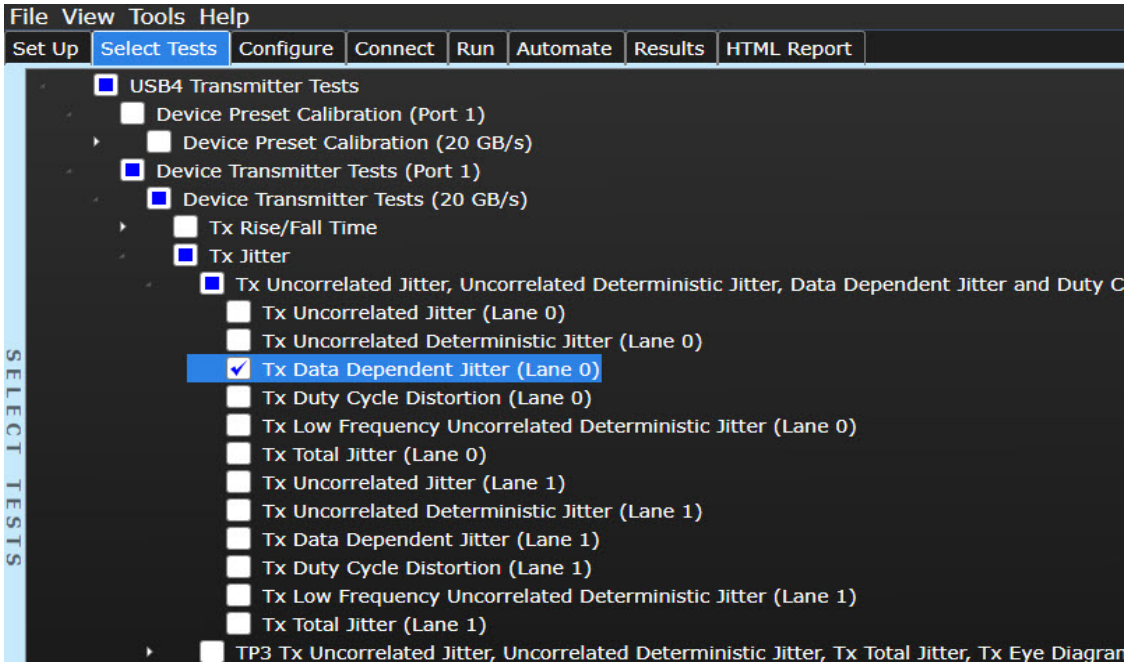


Figure 185 Selecting the Tx Data Dependent Jitter tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2 Perform measurements with:
   a Reference CDR based on the 2^{nd} order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   b Oscilloscope with a minimum bandwidth of 21 GHz
3 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Pattern length – Periodic
   c Jitter Separation method must be suitable for cross-talk on the signal
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Evaluate 40 Mpts per channel when using 80 GSa/s. For higher sample rates, use memory depth in the same ratio to 40 Mpts
   f Referenced to 1E-13 statistics
4 Capture the DDJ result (same as ISI over the Oscilloscope).
5 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If DDJ > 0.21 UI_{p-p}, the status of test is FAIL.x

Test References

See

- *Universal Serial Bus 4 (USB Type-C) Specification Version 1.00 (Table 3-8)*

Tx Duty Cycle Distortion

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Duty Cycle Distortion Test is to confirm that the transmitter Deterministic Jitter Associated by Duty-Cycle-Distortion Jitter falls within the limits of the specification.

Test Pass Requirement

Duty-Cycle-Distortion (DCD) ≤ 0.03 UIp-p (Refer to Table 8 on page 85).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 174 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter, Data Dependent Jitter and Duty Cycle Distortion* are checked.

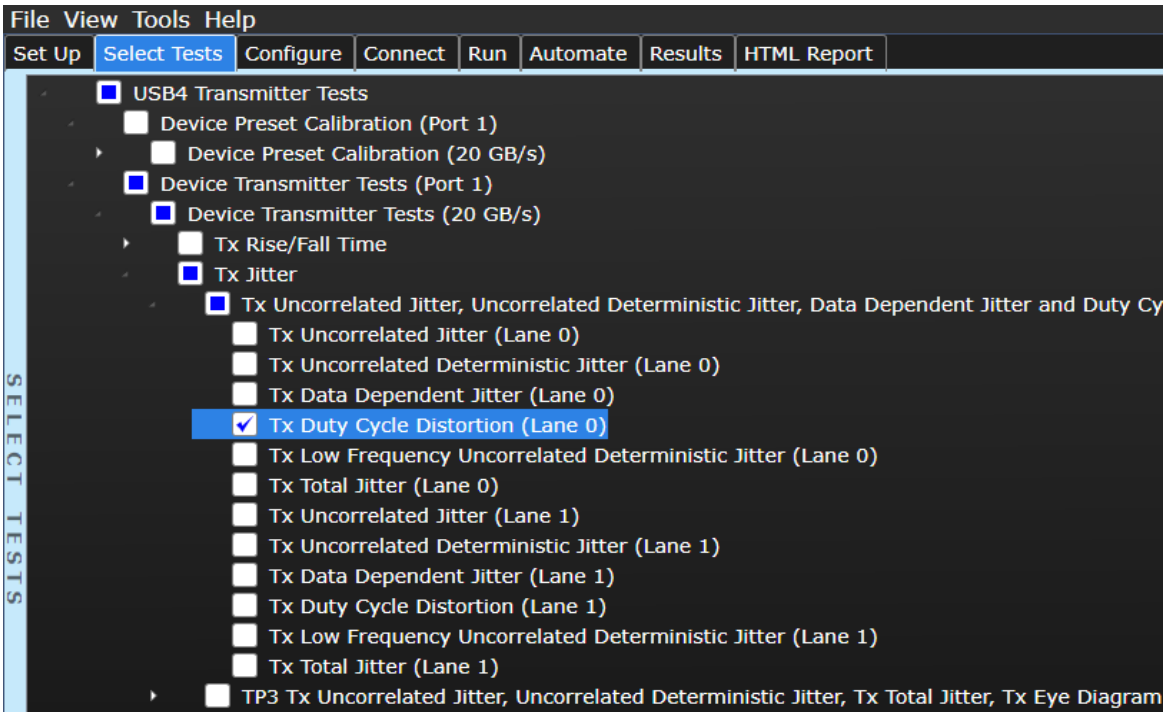


Figure 186 Selecting the Tx Duty Cycle Distortion tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2 Perform measurements with:
   a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   b Oscilloscope with a minimum bandwidth of 21GHz
3 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Pattern length – Periodic
   c Jitter Separation method must be suitable for cross-talk on the signal
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Evaluate 40 Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ratio to 40 Mpts.
4 Capture the DCD result.
5 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If DCD > 0.03 UIp-p, the status of test is FAIL.

Test References

See

Universal Serial Bus 4 (USB Type-C) Specification Version 1.00 (Table 3-8)

Tx Low Frequency Uncorrelated Deterministic Jitter

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Low Frequency Uncorrelated Deterministic Jitter Test is to confirm that the Low Frequency Uncorrelated Deterministic Jitter of the transmitter is within the limits of the specification.

Test Pass Requirement

Low Frequency Uncorrelated Deterministic Jitter (UDJ_LF) $\leq$ 0.07 UI_{p-p} (Refer to Table 8 on page 85).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 174 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter, Data Dependent Jitter and Duty Cycle Distortion* are checked.

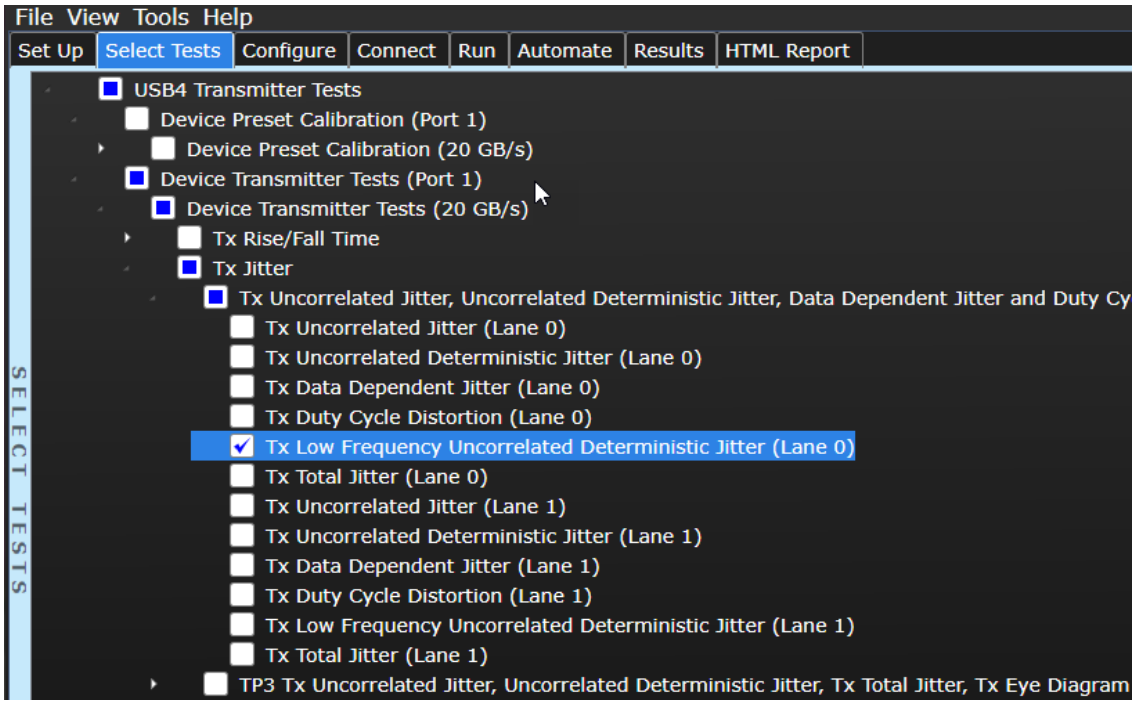


Figure 187 Selecting the Tx Low Frequency Uncorrelated Deterministic Jitter tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2 Perform measurements with:
   a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 0.5 MHz and damping factor of 0.94.
   b Apply 2^{nd} order Low-Pass-Filter with 3 dB cut-off at 2MHz; no average and no interpolation to be used
   c Oscilloscope with a bandwidth of 21GHz
3 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Pattern length – Periodic
   c Jitter Separatio method must be suitable for cross-talk on the signal
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Evaluate 40 Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ratio to 40 Mpts
4 Capture the UDJ_LF result.
5 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If UDJ_LF > 0.07 UI_{p-p}, the status of test is FAIL.

Test References

See

- *Universal Serial Bus 4 (USB Type-C) Specification Version 1.00 (Table 3-8)*

Tx Total Jitter

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Total Jitter Test is to confirm that the Total Jitter of the transmitter is within the limits of the specification.

Total Jitter (TJ) is defined as the sum of all "deterministic" components plus 14.7 times the Random Jitter (RJ) RMS. 14.7 is the factor that accommodates a Bit Error Ratio value of 1 x 10^{-13}.

Test Pass Requirement

Total Jitter (TJ) $\leq$ 0.46 UI_{p-p} (Refer to Table 8 on page 85).

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see Figure 174 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.
2. Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.
3. Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Total Jitter* are checked.

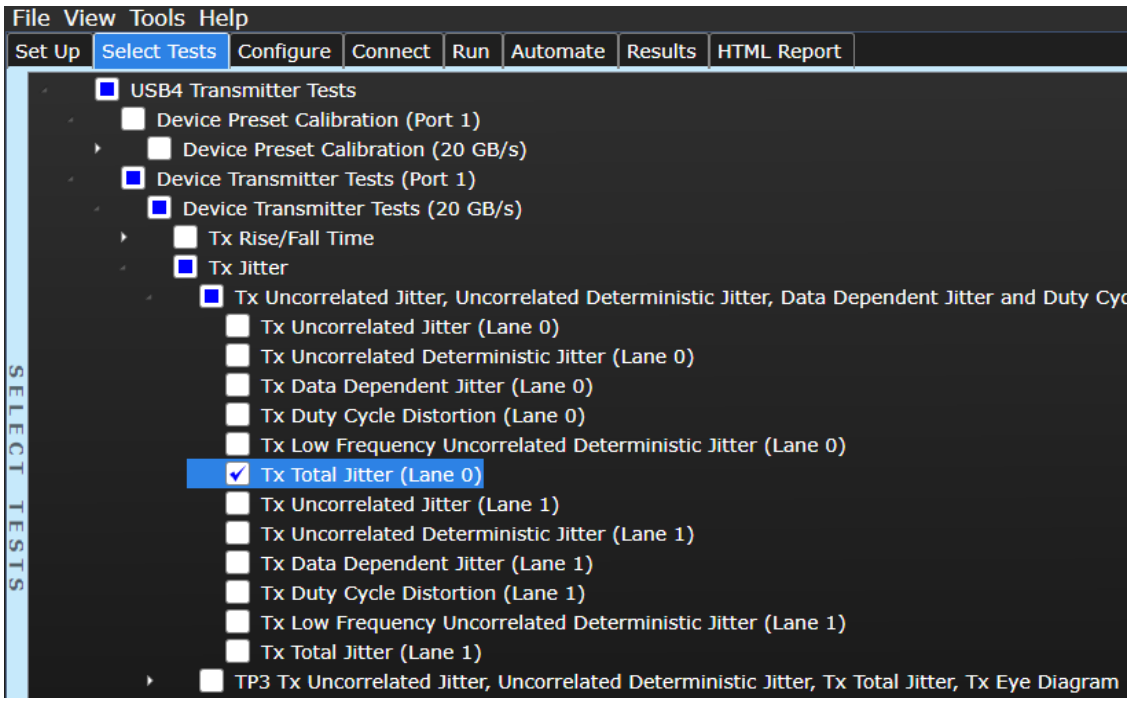


Figure 188 Selecting the Tx Total Jitter tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2 Perform measurements with:
   a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94
   b Oscilloscope with a minimum bandwidth of 21GHz
3 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Pattern length – Periodic
   c Jitter Separation method must be suitable for cross-talk on the signal
   d Evaluate 40 Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ratio to 40 Mpts
   e Adjust vertical scale such that the signal fits within the Oscilloscope's display.
   f Referenced to 1E-13 statistics.
4 Capture the values of Total Jitter (TJ) and Deterministic Jitter (DJ).
5 If TJ > 0.46 UI_{p-p}, perform the following steps:
   a Configure the DUT transmitter to output alternating square pattern of one 0's and one 1's on all lanes with SSC enabled. (The pattern is SQ2 instead of PRBS15).
   b Perform measurements with:
   - Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94
   - Oscilloscope with a minimum bandwidth of 21GHz

   c Capture the waveform and process it with the Digital Oscilloscope:
   - Sampling Rate $\geq$ 80 GSa/s
   - Pattern length – Periodic
   - Jitter Separation method must be suitable for cross-talk on the signal
   - Evaluate 40 Mpts per channel when using 80 GSa/s. For higher sample rates, use memory depth in the same ratio to 40 Mpts
   - Adjust vertical scale such that the signal fits within the Oscilloscope's display.
   - Referenced to 1E-13 statistics.

   d Capture the Random Jitter (RJ) result.
   e Calculate TJ using the equation:

$$TJ = DJ + 14.7 * RJ \text{ (DJ from \#4; PRBS15 and RJ from \#5d; SQ2)}$$

6 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If TJ > 0.46 UI_{p-p}, the status of test is FAIL.

Test References

See

Universal Serial Bus 4 (USB Type-C) Specification Version 1.00 (Table 3-8)

Tx Uncorrelated Jitter TP3

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Uncorrelated Jitter TP3 Test is to confirm that the Uncorrelated Jitter [Deterministic Jitter (DJ) and Random Jitter (RJ) components] at point TP3 of the transmitter is within the limits of the specification.

Test Pass Requirement

Uncorrelated Jitter (UJ_{TP3}) $\leq$ 0.31 UI_{p-p} (Refer to Table 9 on page 86).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 174 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter, Data Dependent Jitter and Duty Cycle Distortion* are checked.

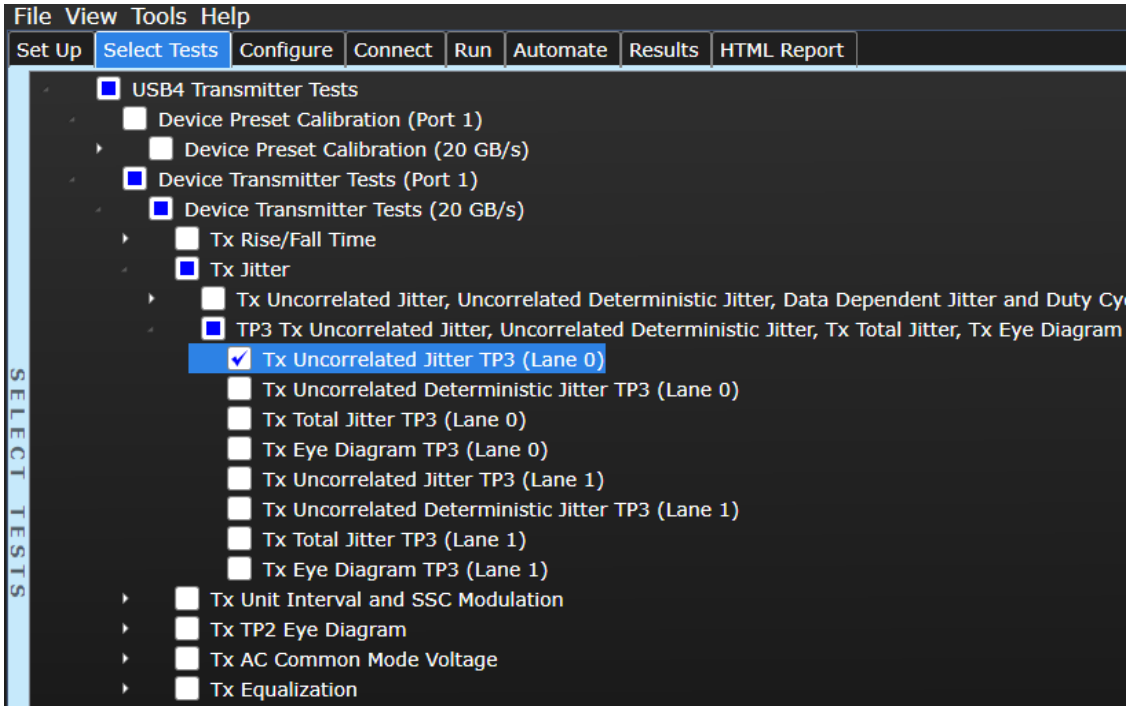


Figure 189 Selecting the Tx Uncorrelated Jitter TP3 tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2 Embed the Type-C cable in the Oscilloscope. For Gen 3 systems, use TP3_EQ embedding file *USB_0p8m.s4p*.
3 De-embed the cables from the test fixture to the Oscilloscope.

NOTE CTLE value is handled in the SigTest tool.

4 Perform measurements with:
   a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   b Oscilloscope with a minimum bandwidth of 21GHz
5 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Pattern length – Periodic
   c Jitter Separatio method must be suitable for cross-talk on the signal
   d Evaluate 40 Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ratio to 40 Mpts
   e Adjust vertical scale such that the signal fits within the Oscilloscope's display
6 Capture the values of Total Jitter (TJ_{TP3}) and Data Deterministic Jitter (DDJ_{TP3}).
7 Capture the UJ_{TP3} result (same as BUJ over the Oscilloscope).
8 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If $UJ_{TP3} > 0.31\ UI_{p-p}$, the status of test is FAIL.

Test References

See

- *Universal Serial Bus 4 (USB Type-C) Specification Version 1.00 (Table 3-9)*

Tx Uncorrelated Deterministic Jitter TP3

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Uncorrelated Deterministic Jitter TP3 Test is to confirm that the Uncorrelated Deterministic Jitter at point TP3 of the transmitter is within the limits of the specification.

Test Pass Requirement

Deterministic Jitter that is uncorrelated to the transmitted data (UDJ_{TP3}) $\leq$ 0.17 UI_{p-p} (Refer to Table 9 on page 86).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 174 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Uncorrelated Jitter, Uncorrelated Deterministic Jitter, Data Dependent Jitter and Duty Cycle Distortion* are checked.

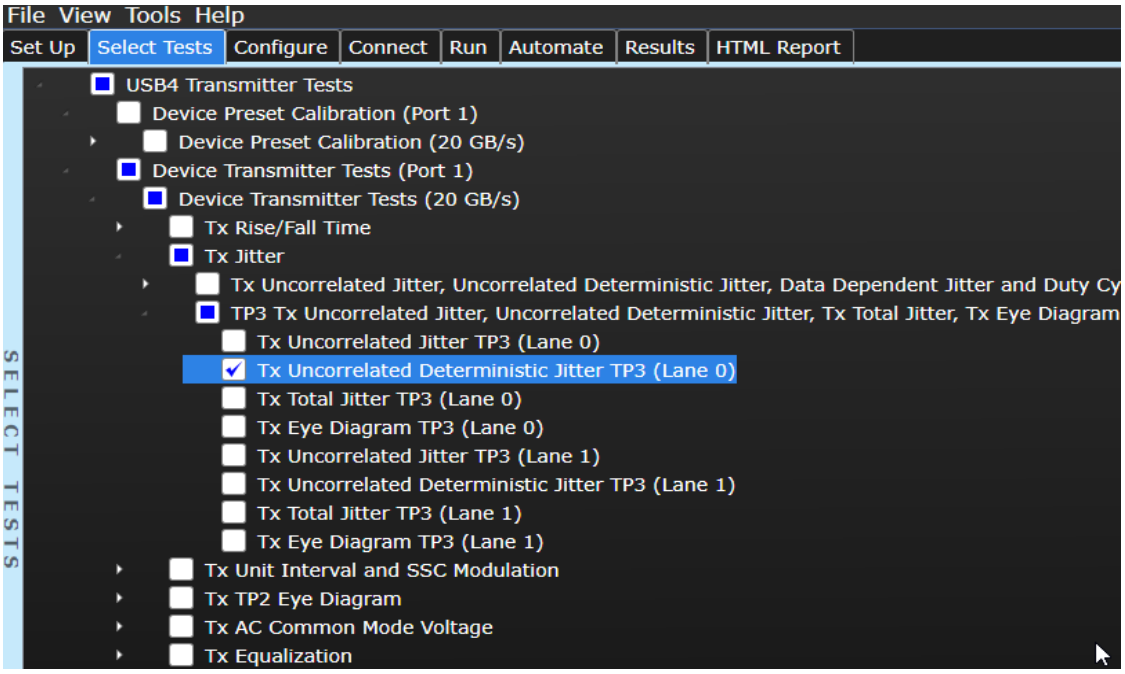


Figure 190 Selecting the Tx Uncorrelated Deterministic Jitter TP3 tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2 Embed the Type-C cable in the Oscilloscope. For Gen 3 systems, use TP3_EQ embedding file *USB_0p8m.s4p*.
3 De-embed the cables from the test fixture to the Oscilloscope.

NOTE CTLE value is handled in the SigTest tool.

4 Perform measurements with:
   a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   b Oscilloscope with a minimum bandwidth of 21GHz
5 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Pattern length – Periodic
   c Jitter Separation method must be suitable for cross-talk on the signal
   d Evaluate 40 Mpts per channel when using 80 GSa/s. For higher sample rates, use memory depth in the same ratio to 40 Mpts
   e Adjust vertical scale such that the signal fits within the Oscilloscope's display
6 Capture the values of Total Jitter (TJ_{TP3}) and Data Deterministic Jitter (DDJ_{TP3}).
7 Capture the UDJ_{TP3} result (same as BUJ over the Oscilloscope).
8 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If $UDJ_{TP3} > 0.17\ UI_{p-p}$, the status of test is FAIL.

Test References

See

Universal Serial Bus 4 (USB Type-C) Specification Version 1.00 (Table 3-9)

Tx Total Jitter TP3

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Total Jitter TP3 Test is to confirm that the Total Jitter at point TP3 of the transmitter is within the limits of the specification.

Total Jitter (TJ) is defined as the sum of all "deterministic" components plus 14.7 times the Random Jitter (RJ) RMS. 14.7 is the factor that accommodates a Bit Error Ratio value of $1x10^{-13}$.

Test Pass Requirement

Total Jitter (TJ_{TP3}) $\leq$ 0.60 UI_{p-p} (Refer to Table 9 on page 86).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 174 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Total Jitter* are checked.

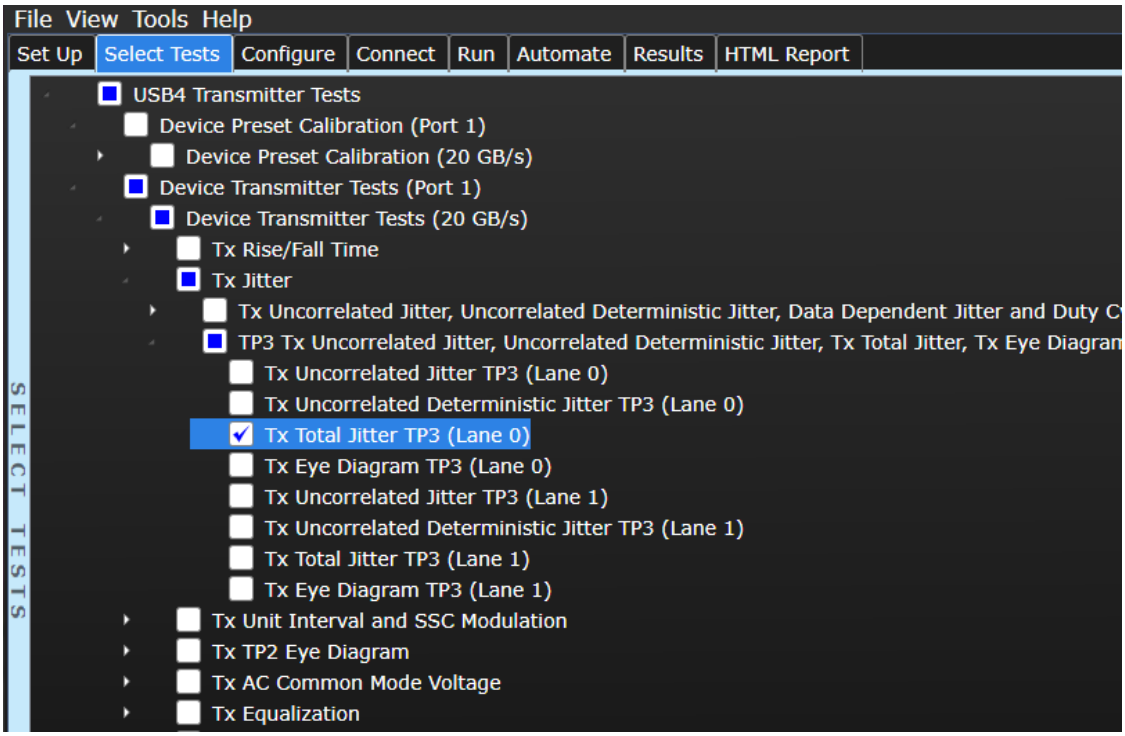


Figure 191 Selecting the Tx Total Jitter TP3 tests

Test Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled.
2 Embed the Type-C cable in the Oscilloscope. For Gen 3 systems, use TP3_EQ embedding file *USB_0p8m.s4p*.
3 De-embed the cables from the test fixture to the Oscilloscope.

NOTE CTLE value is handled in the SigTest tool.

4 Perform measurements with:
   a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and no interpolation to be used
   b Oscilloscope with a bandwidth of 21GHz
5 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Pattern length – Periodic
   c Jitter Separation method must be suitable for cross-talk on the signal
   d Evaluate 40 Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ratio to 40 Mpts
   e Adjust vertical scale such that the signal fits within the Oscilloscope's display
   f Referenced to 1E-13 statistics
6 Capture the values of Total Jitter (TJ_{TP3}) and Deterministic Jitter (DJ_{TP3}).
7 If $TJ_{TP3} > 0.60\ UI_{p-p}$, perform the following steps:
   a Configure the DUT transmitter to output alternating square pattern of one 0's and one 1's on all lanes with SSC enabled. (The pattern is SQ2 instead of PRBS15).
   b Perform measurements with:
   - Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94
   - Oscilloscope with a minimum bandwidth of 21GHz

   c Capture the waveform and process it with the Digital Oscilloscope:
   - Sampling Rate $\geq$ 80 GSa/s
   - Pattern length – Periodic
   - Jitter Separatio method must be suitable for cross-talk on the signal
   - Evaluate 40 Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ratio to 40 Mpts
   - Adjust vertical scale such that the signal fits within the Oscilloscope's display.
   - Referenced to 1E-13 statistics.

   d Capture the Random Jitter (RJ_{TP3}) result.
   e Calculate TJ_{TP3} using the equation:

$$TJ_{TP3} = DJ_{TP3} + 14.7 * RJ_{TP3}$$ (DJ_{TP3} from #7; PRBS15 and RJ_{TP3} from #8d; SQ2)

8 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If $TJ_{TP3} > 0.60\ UI_{p-p}$, the status of test is FAIL.

Test References

See

Universal Serial Bus 4 (USB Type-C) Specification Version 1.00 (Table 3-9)

Tx Eye Diagram TP3

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Eye Diagram TP3 Test is to confirm that the differential signal on each USB differential lane has an eye opening that meets or exceeds the limits for eye opening in the specification.

Test Pass Requirement

The eye diagram at TP3 should meet the conditions depicted in Figure 192.

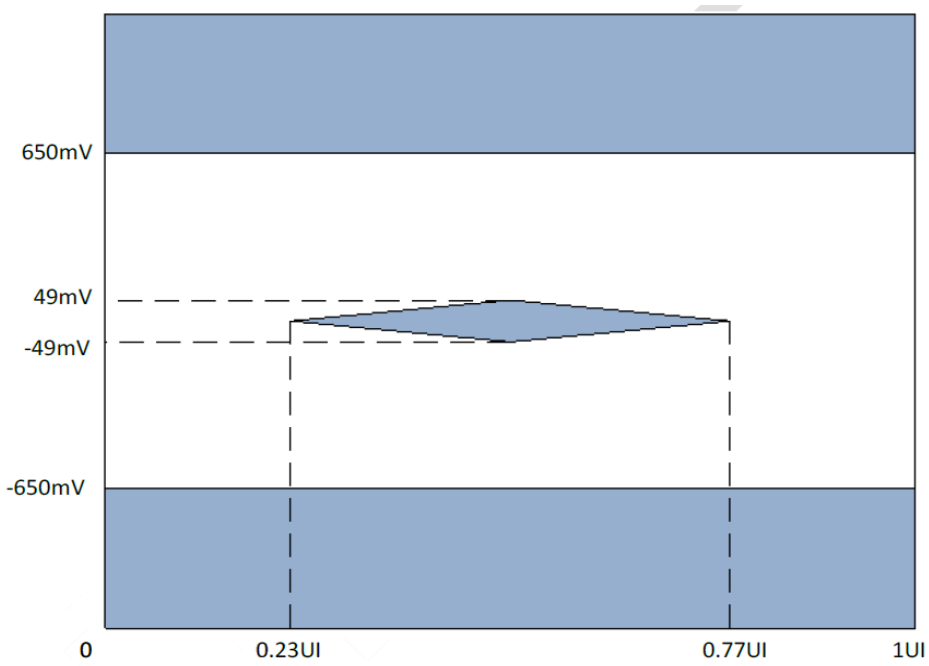


Figure 192 Pass Condition for Tx Eye Diagram TP3 Tests

(Refer to Table 9 on page 86 and Figure 192 on page 384).

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see "Transmitter TP2/TP3 Test Setup" on page 348 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.
2. Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.
3. Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Eye Diagram* are checked.

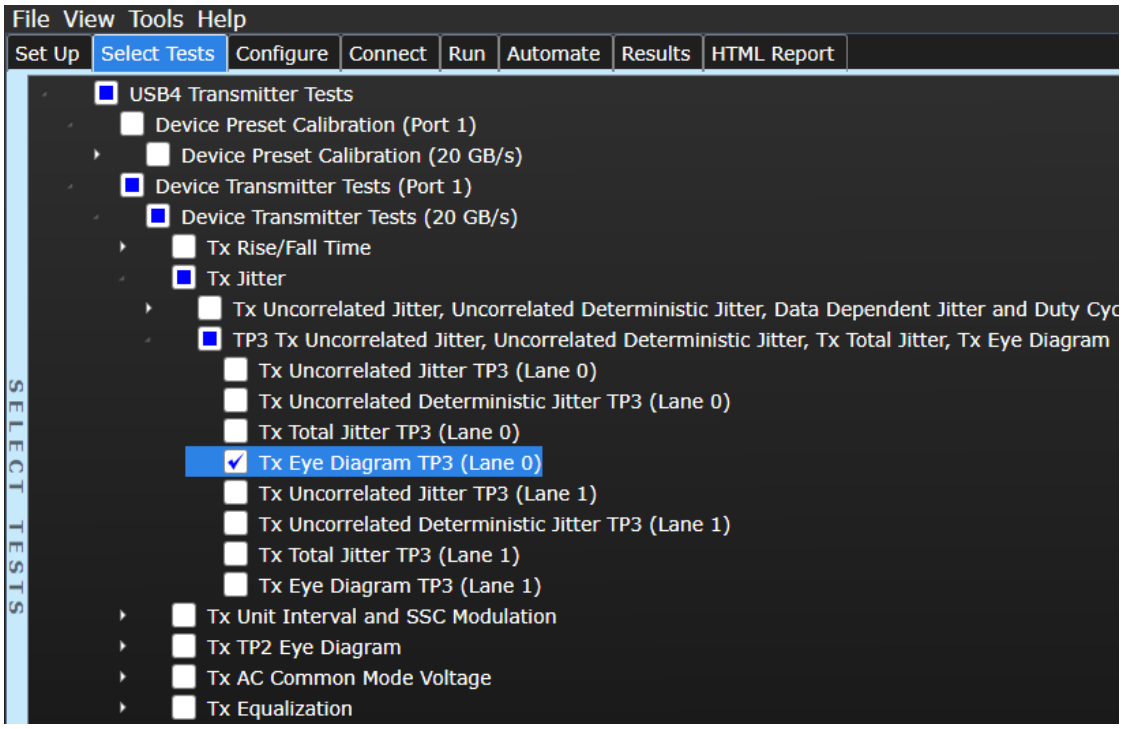


Figure 193 Selecting the Tx Eye Diagram TP3 tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2 Embed the Type-C cable in the Oscilloscope. For Gen 3 systems, use TP3_EQ embedding file *USB_0p8m.s4p*.
3 De-embed the cables from the test fixture to the Oscilloscope.

NOTE CTLE and DFE values are handled in the SigTest tool.

4 Perform measurements with:
   a Change from no interpolation to X16 a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and X16 interpolation to be used.
   b Oscilloscope with a minimum bandwidth of 21GHz
5 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Adjust vertical and horizontal scale such that the signal fits within the Oscilloscope's display
   c Accumulate at 1E6 UI
6 Compare the data eye to the TP3 eye diagram mask. Check for conditions described in the section "Expected / Observable Results".
7 Repeat the test for the remaining USB lanes.

Expected / Observable Results

i If any part of the waveform exceeds either the high or low maximum voltage (+/-1000mV), the status of the test is FAIL.

ii If any part of the waveform hits the mask, the status of the test is FAIL.

Test References

See

- *Universal Serial Bus 4 (USB Type-C) Specification Version 1.00 (Table 5-9)*

Tx Minimum Unit Interval, Min/Max

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Unit Interval Test is to confirm that the data rate, under all conditions, does not exceed the minimum or maximum limits of the specification.

Test Pass Requirement

Tx Minimum Unit Interval Min

Minimum Unit Interval, Min (Device, 20 Gb/s) >= 49.9850 ps

Tx Minimum Unit Intreval Max

Minimum Unit Interval, Max (Device, 20 Gb/s) <= 50.0150 ps

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 174 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Unit Interval and SSC Down Spread Modulation* are checked.

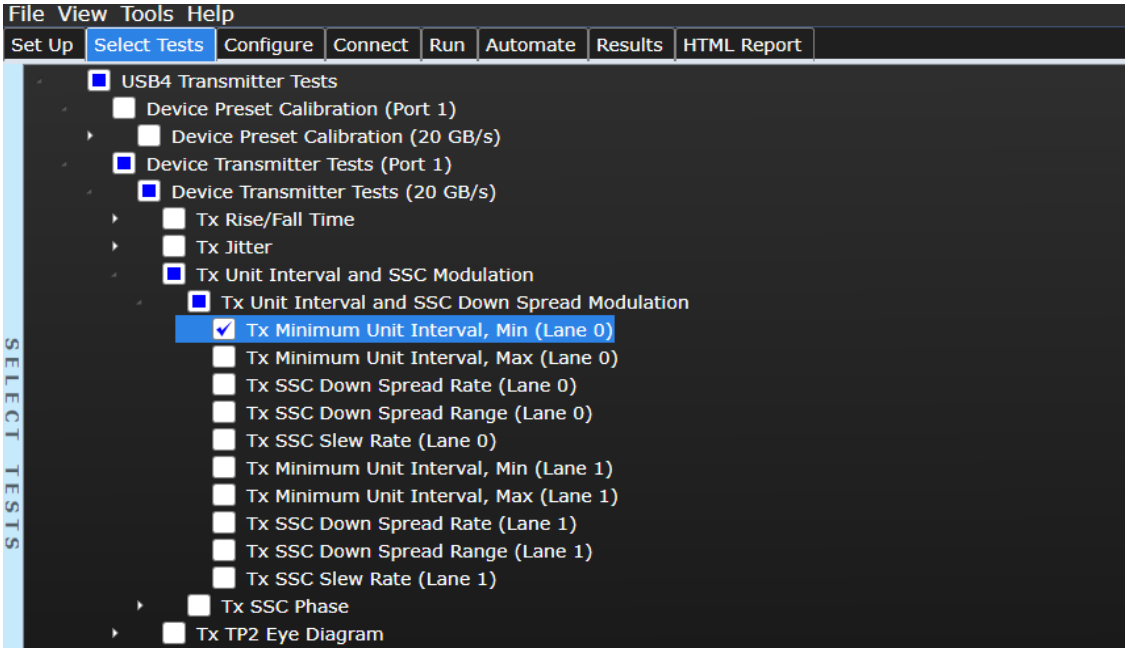


Figure 194 Selecting the Tx Unit Interval tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ratio to 27Mpts
   c No CDR, no average and no interpolation to be used
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Oscilloscope must have a minimum bandwidth of 21GHz
3 Calculate UI dynamically using a uniform moving average filter procedure with a window size of 6000 symbols.
4 Measure the values of both UI_{MAX} and UI_{MIN}.
5 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If $UI_{MAX} > 50.0150$ ps, the status of test is FAIL.

If $UI_{MIN} < 49.9850$ ps, the status of test is FAIL.

Test References

See

- *Universal Serial Bus 4 (USB Type-C) Specification Version 1.00 (Table 3-8)*

Tx SSC Down Spread Rate

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx SSC Down Spread Rate Test is to confirm that the Link clock down-spreading modulation rate is within the limits of the specification.

Test Pass Requirement

30.00 kHz ≤ SSC_Down_Spread_Rate ≤ 33.00 kHz (Refer to Table 3 on page 74).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 174 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Unit Interval and SSC Down Spread Modulation* are checked.

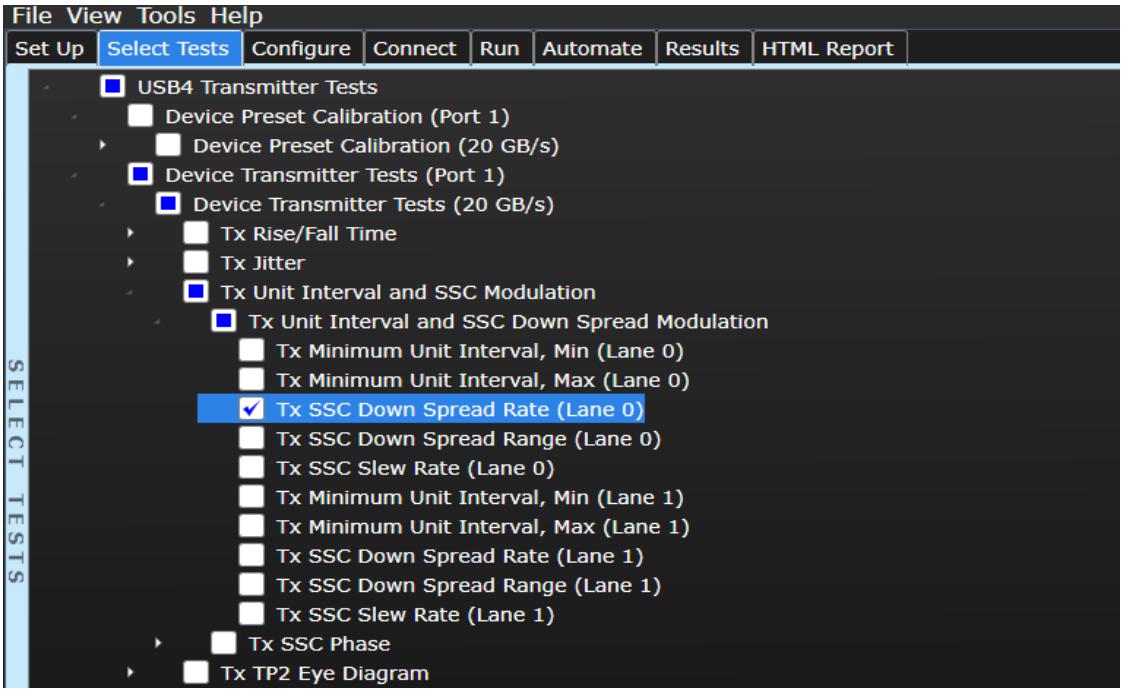


Figure 195 Selecting the Tx SSC Down Spread Rate tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ratio to 27Mpts
   c No CDR, no average and no interpolation to be used
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Oscilloscope must have a minimum bandwidth of 21GHz
3 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If 30.00 kHz > SSC_Down_Spread_Rate > 33.00 kHz, the status of test is FAIL.

Test References

See

- *Universal Serial Bus 4 (USB Type-C) Specification Version 1.00 (Table 3-3)*

Tx SSC Down Spread Range

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx SSC Down Spread Range Test is to confirm that the data down spreading is within the limits of the specification.

Test Pass Requirement

0.4% ≤ SSC_Down_Spread_Range ≤ 0.5% (Refer to Table 3 on page 74).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 174 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Unit Interval and SSC Down Spread Modulation* are checked.

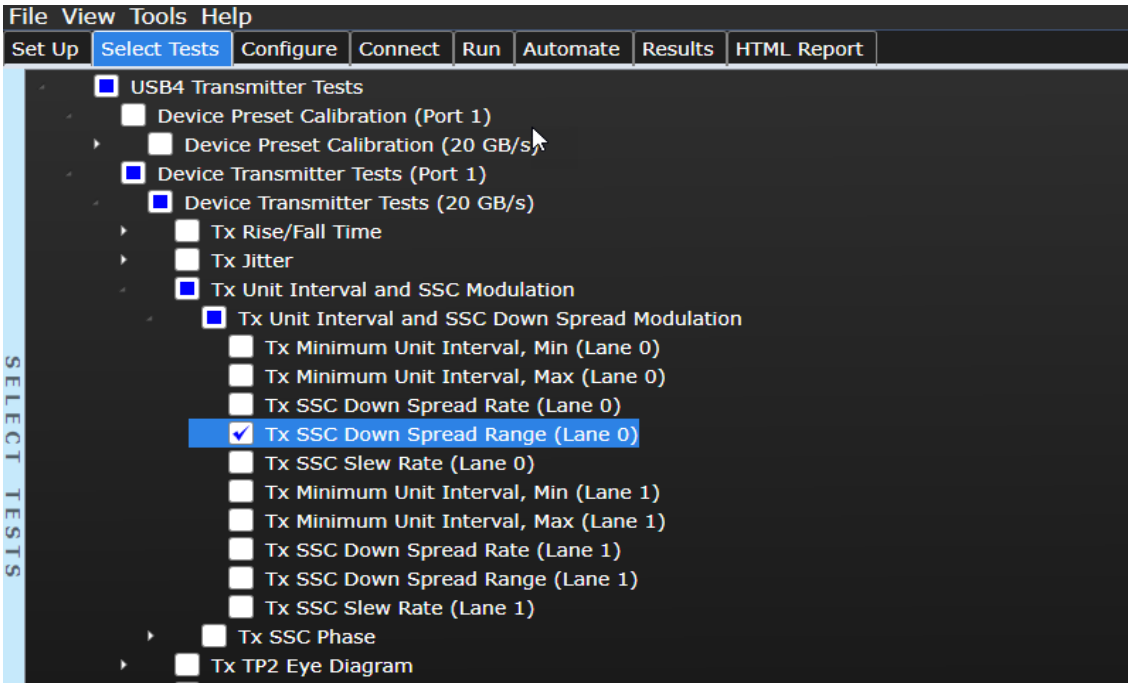


Figure 196 Selecting the Tx SSC Down Spread Range tests

Test Procedure

1. Run the "Tx Eye Diagram TP3" Test as a prerequisite to obtain UI_{MAX} and UI_{MIN}.
2. Use the obtained value of UI_{MAX} and UI_{MIN} to calculate the Deviation percentage:

$$\text{Maximum Deviation} = 100*\{[20G - (1 / UI_{MAX})] / 20G\}$$

$$\text{Minimum Deviation} = 100*\{[20G - (1 / UI_{MIN})] / 20G\}$$

3. Calculate SSC Down Spread Range using the equation:

$$\text{Maximum Deviation - Minimum Deviation}$$

4. Repeat the test for all remaining USB lanes.

Expected / Observable Results

If SSC_Down_Spread_Range > 0.5% or SSC_Down_Spread_Range < 0.4%, the status of test is FAIL.

Test References

See

Universal Serial Bus 4 (USB Type-C) Specification Version 1.00 (Table 3-3).

Tx SSC Slew Rate

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx SSC Slew Rate Test is to confirm that the SSC Slew Rate is within the limits of the specification.

Test Pass Requirement

SSC_Slew_Rate $\leq$ 1250 ppm/µs (Refer to Table 3 on page 74).

Test Setup

1. For the physical connection between the DUT & the Oscilloscope, see Figure 174 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.
2. Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.
3. Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Unit Interval and SSC Down Spread Modulation* are checked.

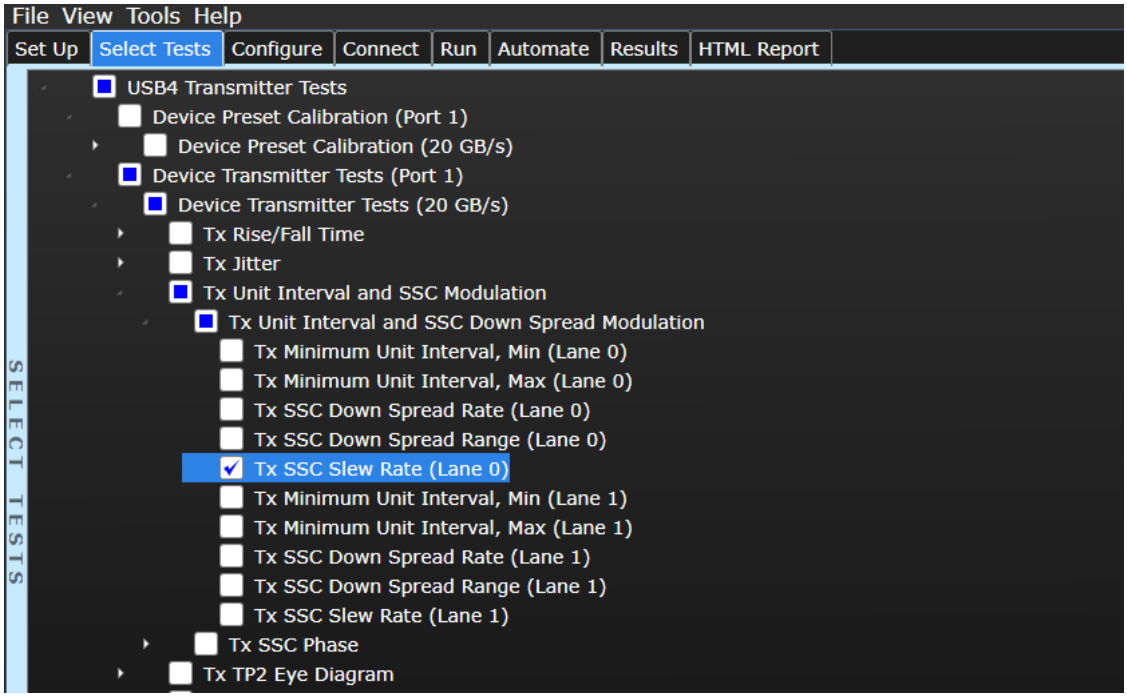


Figure 197 Selecting the Tx SSC Slew Rate tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2 Capture the waveform and post process it with an appropriate software:
   a Sampling Rate $\geq$ 80 GSa/s
   b Evaluate 27 Mpts per channel when using 80 GSa/s. For higher sample rates, use memory depth in the same ratio to 27 Mpts
   c No CDR, no average and no interpolation to be used
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Extract SSC slew rate from the transmitted signal over measurement intervals of 0.5 µs
   f Extract SSC slew rate from the phase information after applying a 2^{nd} order Low-Pass-Filter with 3 dB cut-off at 5 MHz.
   g Oscilloscope must have a minimum bandwidth of 21 GHz
3 SSC_Slew_Rate is measured as the SSC frequency deviation over time while valid data is being transmitted in which 1E-12 bit error rate is required without assuming forward error correction.
4 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If SSC_Slew_Rate > 1250 ppm/µs, the status of test is FAIL.

Test References

See

Universal Serial Bus 4 (USB Type-C) Specification Version 1.00 (Table 3-3)

Tx SSC Phase Deviation

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx SSC Phase Deviation Test is to confirm that the SSC Phase Deviation is within the limits of the specification.

Test Pass Requirement

2.50 ns p-p ≤ SSC_Phase_Deviation ≤ 22.00 ns p-p (Refer to Table 3 on page 74).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 174 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx SSC Phase* are checked.

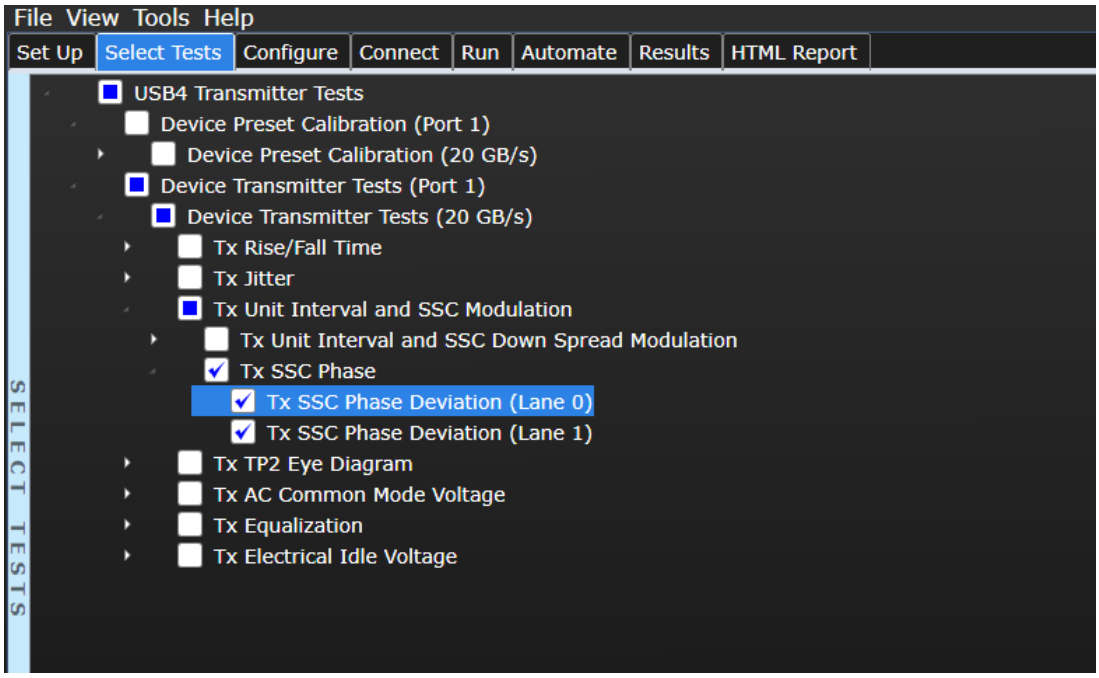


Figure 198 Selecting the Tx SSC Phase Deviation tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2 Capture the waveform and process it with the Digital Oscilloscope's software:
   a Sampling Rate $\geq$ 80 GSa/s
   b Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ratio to 27Mpts
   c No CDR, no average and no interpolation to be used
   d Adjust vertical scale such that the signal fits within the Oscilloscope's display
   e Oscilloscope must have a minimum bandwidth of 21GHz
3 Extract the SSC Phase Deviation from the transmitted signal.
4 Extract the SSC Phase Deviation from the phase jitter after applying a 2^{nd} order low-pass filter with 3dB point at 5 MHz.
5 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If 2.50 ns p-p > SSC_Phase_Deviation > 22.00 ns p-p the status of test is FAIL.

Test References

See

- *Universal Serial Bus 4 (USB Type-C) Specification Version 1.00 (Table 3-3)*

Tx Eye Diagram

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Eye Diagram Test is to confirm that the differential signal on each USB differential lane has an eye opening that meets or exceeds the limits for eye opening in the specification.

Test Pass Requirement

The eye diagram should meet the conditions depicted in Figure 199.

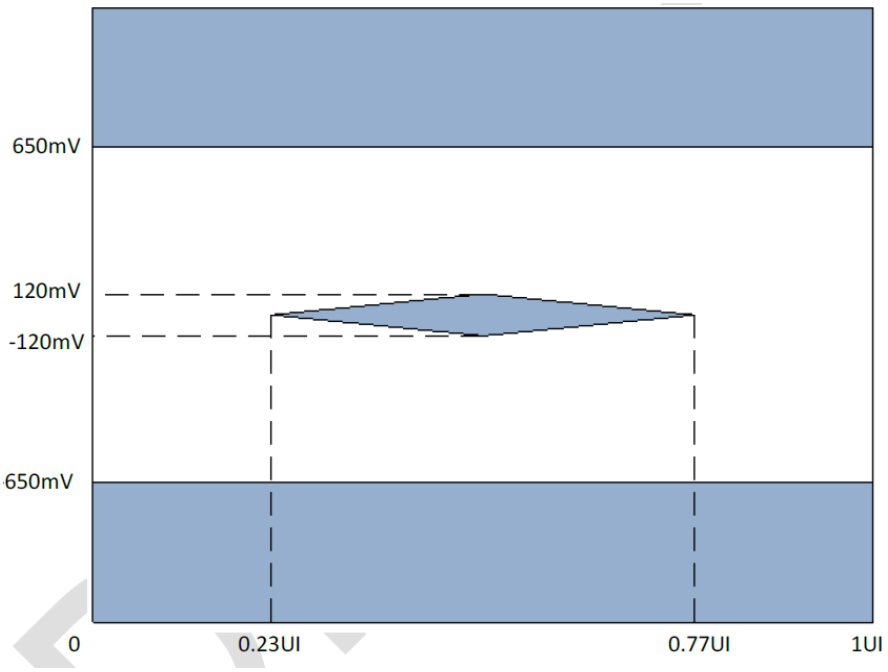


Figure 199 Pass Condition for Tx Eye Diagram Tests

(Refer to Table 8 on page 85 and Figure 199 on page 397).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see "Transmitter TP2/TP3 Test Setup" on page 348 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Eye Diagram* are checked.

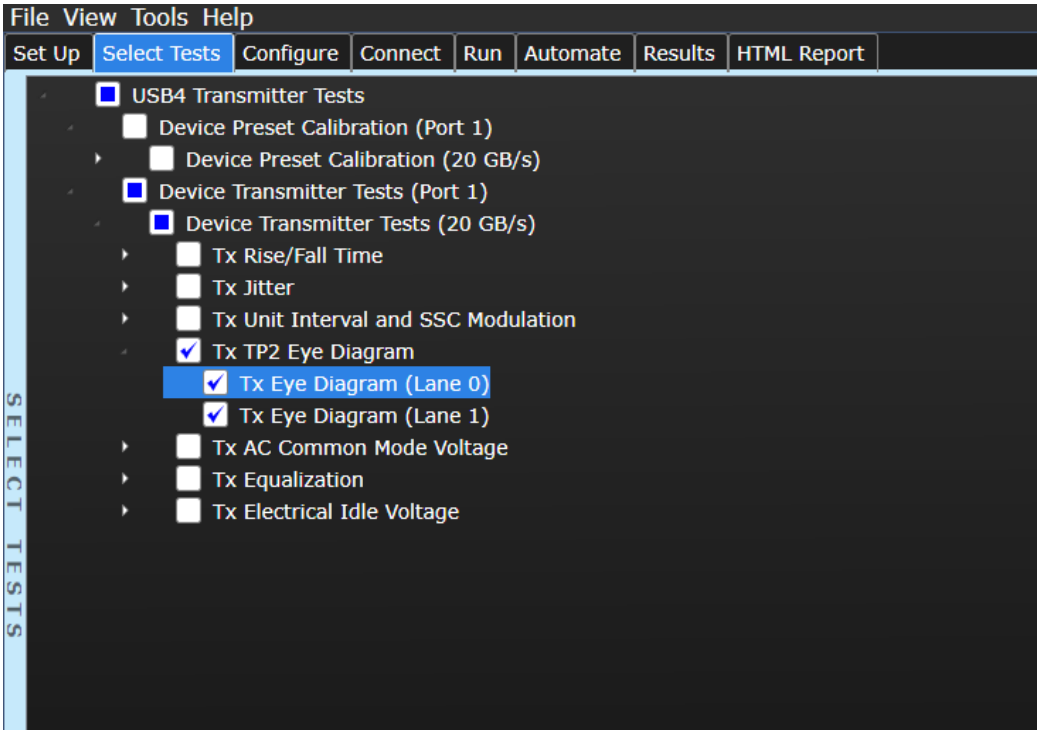


Figure 200 Selecting the Tx Eye Diagram tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2 Perform measurements with:
   a Perform measurements with: Change from no interpolation to X16 a Reference CDR based on the 2nd order PLL response, which in turn, must drive a High-Pass-Filter (HPF) rejection mask with 3 dB bandwidth at 5 MHz and damping factor of 0.94; no average and X16 interpolation to be used.
   b Oscilloscope with a minimum bandwidth of 21GHz
3 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Adjust vertical scale such that the signal fits within the Oscilloscope's display
   c Measured at 1E6 UI
4 Compare the data eye to the TP1 eye diagram mask. Check for conditions described in the section "Expected / Observable Results".
5 Repeat the test for the remaining USB lanes.

Expected / Observable Results

   i If any part of the waveform exceeds either the inner or outer height voltage (+/- 700mV), the status of the test is FAIL.
   ii If any part of the waveform hits the mask, the status of the test is FAIL.

Test References

See

- Universal Serial Bus 4 (USB Type-C) Specification Version 1.00 (Table 5-8)

Tx AC Common Mode Voltage

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx AC Common Mode Voltage Test is to confirm that the transmitter common mode on the USB differential signals is within the limits of the specification.

Test Pass Requirement

TX AC Common Mode Voltage $\leq$ 100 mV_{p-p} (Refer to Table 8 on page 85).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 174 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx AC Common Mode Voltage* are checked.

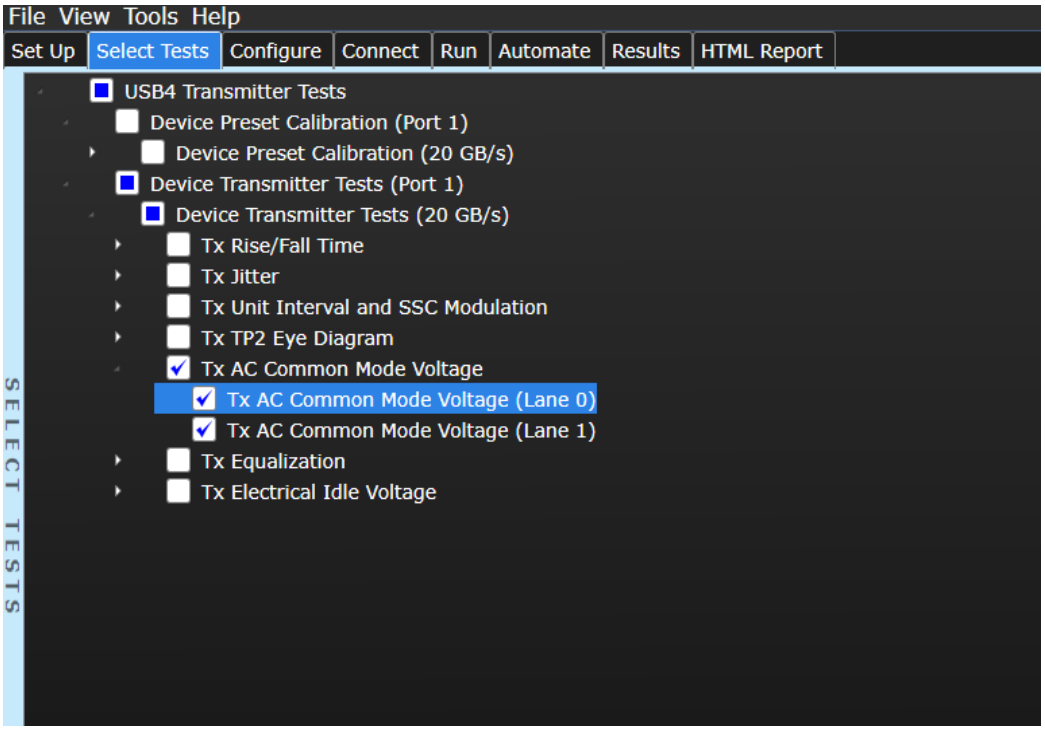


Figure 201 Selecting the Tx AC Common Mode Voltage tests

Test Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled.
2 Capture the waveform and process it with the Digital Oscilloscope:
   a Sampling Rate $\geq$ 80 GSa/s
   b Evaluate 27Mpts per channel when using 80GSa/s. For higher sample rates, use memory depth in the same ratio to 27Mpts
   c No CDR, no average and no interpolation to be used
   d Oscilloscope must have a bandwidth of 21±1GHz
3 Calculate the AC Common Mode Voltage (V_{AC-CM}) using the equation:

$$V_{AC-CM} = (V_{TX-P} + V_{TX-N}) / 2$$

4 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If $V_{AC-CM} > 100.00\ mV_{p-p}$, the status of test is FAIL.

Test References

See

Universal Serial Bus 4 (USB Type-C) Specification Version 1.00 (Table 3-8)

Tx Equalization Tests

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Tx Equalization Tests is to confirm that the transmitter equalization is within the limits of the specification. The Tx Equalization Tests are further divided into three tests, namely:

- Tx Equalization Preshoot
- Tx Equalization Deemphasis
- Tx Swing Preset 15

Test Pass Requirement

Transmitter Swing: 3.5 ± 1dB (for preset 15 only)

Pre-shoot, De-Emphasis: ± 1dB for the following presets:

Table 13 Transmitter Equalization Presets

Preset Number	Pre-Shoot	De-Emphasis	Informative Filter Coefficients		
			C_{-1}	C_0	C_1
0	0	0	0	1	0
1	0	-1.9	0	0.90	-0.10
2	0	-3.6	0	0.83	-0.17
3	0	-5.0	0	0.78	-0.22
4	0	-8.4	0	0.69	-0.31
5	0.9	0	-0.05	0.95	0
6	1.1	-1.9	-0.05	0.86	-0.09
7	1.4	-3.8	-0.05	0.79	-0.16
8	1.7	-5.8	-0.05	0.73	-0.22
9	2.1	-8.0	-0.05	0.68	-0.27
10	1.7	0	-0.09	0.91	0
11	2.2	-2.2	-0.09	0.82	-0.09
12	2.5	-3.6	-0.09	0.77	-0.14
13	3.4	-6.7	-0.09	0.69	-0.22
14	3.6	0	-0.17	0.83	0
15	1.7	-1.7	-0.05	0.55	-0.05

(Refer to Table 5 on page 81).

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 174 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group *Tx Equalization* are checked.

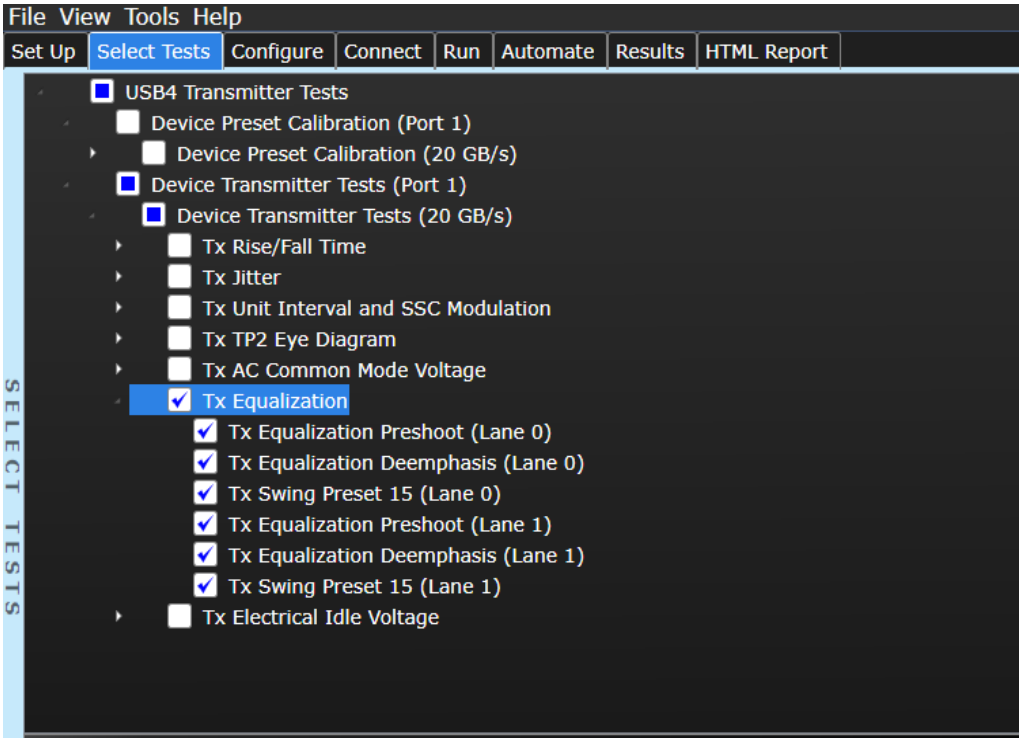


Figure 202 Selecting the Tx Equalization tests

4 Under the **Configure** tab of the Test Application, select **ALL** for the configuration Variable “Tx Equalization” to run the tests for preset numbers P0 to P15.

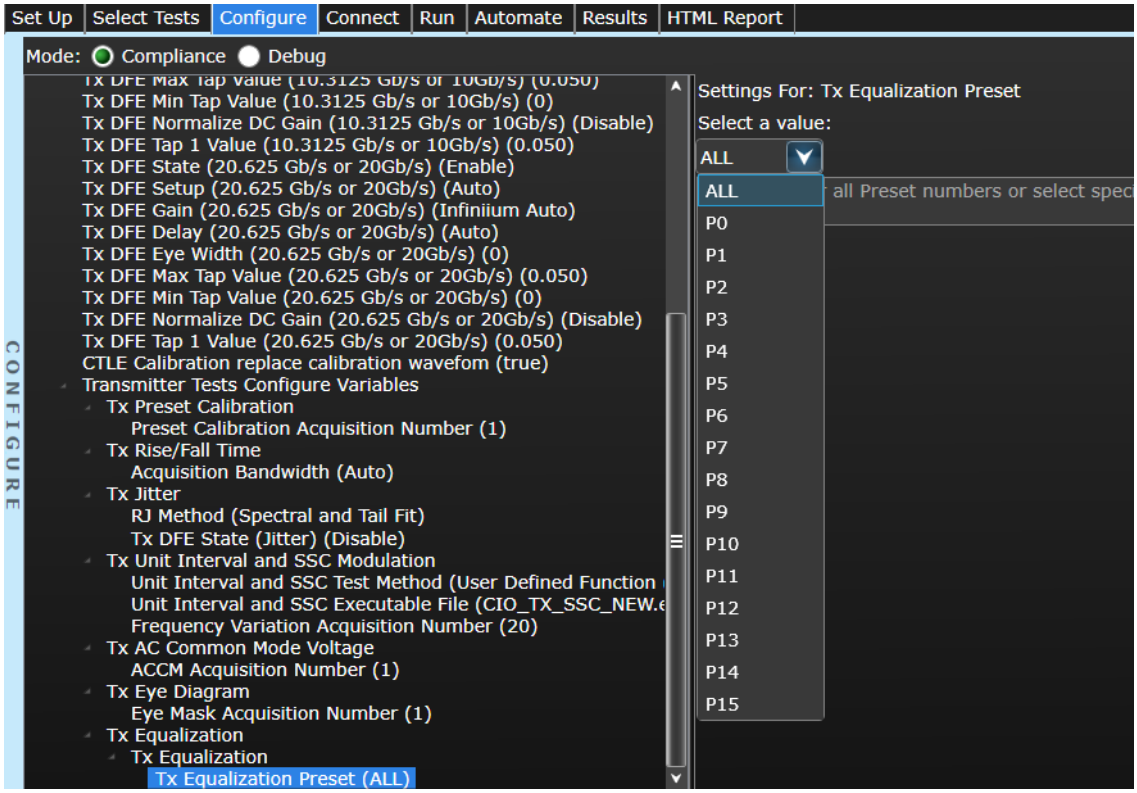


Figure 203 Configuring Tx Equalization Preset Variable

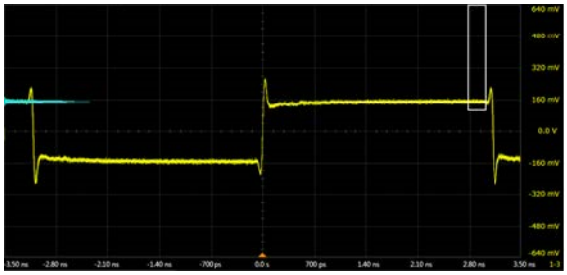
Test Procedure

1 Set Preset 0 (P0).

2 Configure the DUT transmitter to output alternating square pattern of 64 0’s and 64 1’s on all lanes with SSC enabled along with both pre-shoot and de-emphasis enabled.

3 Adjust vertical scale such that the signal fits within the Oscilloscope’s display.

4 Average one cycle using 150 cycles; no CDR and no interpolation to be used. Oscilloscope must have a minimum bandwidth of 21GHz.



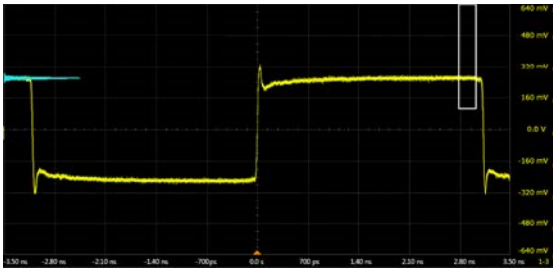
5 Measure differential amplitude voltage (V_1) for bits 57 to 62 using the equation:

$$V_1 = [|V_{bits(57\text{-}62)} \text{ (64 bits of 1's)} - V_{bits(57\text{-}62)} \text{ (64 bits of 0's)}|]$$

6 Configure the DUT transmitter to output alternating square pattern of 64 0's and 64 1's on all lanes with SSC enabled along with de-emphasis enabled but no pre-shoot.

7 Adjust vertical scale such that the signal fits within the Oscilloscope's display.

8 Average one cycle using 150 cycles; no CDR and no interpolation to be used. Oscilloscope must have a minimum bandwidth of 21GHz.



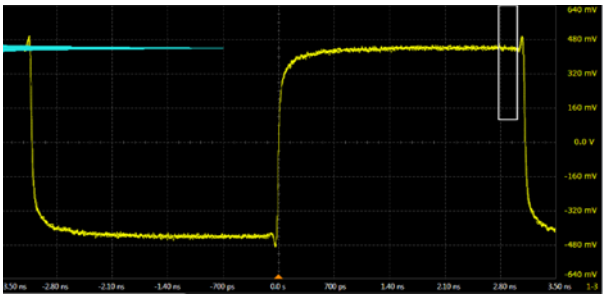
9 Measure differential amplitude voltage (V_2) for bits 57 to 62 using the equation:

$$V_2 = [|V_{bits(57\text{-}62)} \text{ (64 bits of 1's)} - V_{bits(57\text{-}62)} \text{ (64 bits of 0's)}|]$$

10 Configure the DUT transmitter to output alternating square pattern of 64 0's and 64 1's on all lanes with SSC enabled along with pre-shoot enabled but no de-emphasis.

11 Adjust vertical scale such that the signal fits within the Oscilloscope's display.

12 Average one cycle using 150 cycles; no CDR and no interpolation to be used. Oscilloscope must have a minimum bandwidth of 21GHz.



13 Measure differential amplitude voltage (V_3) for bits 57 to 62 using the equation:

$$V_3 = [|V_{bits(57\text{-}62)} \text{ (64 bits of 1's)} - V_{bits(57\text{-}62)} \text{ (64 bits of 0's)}|]$$

Set Pre-Shoot to be $20 * \log_{10} [V_2/V_1]$

Set De-Emphasis to be $20 * \log_{10} [V_1/V_3]$

14 Repeat steps 2 to 10 for all Presets defined in Table 13.

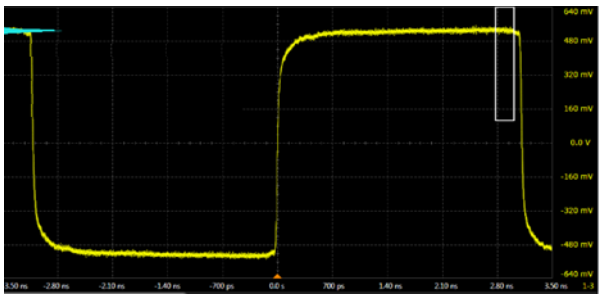
15 Check for PASS/FAIL conditions for both Pre-shoot and De-emphasis.

16 Set the DUT to Preset 0 (P0).

17 Configure the DUT transmitter to output alternating square pattern of 64 0's and 64 1's on all lanes with SSC enabled but with both pre-shoot and de-emphasis disabled.

18 Adjust vertical scale such that the signal fits within the Oscilloscope's display.

19 Average one cycle using 150 cycles; no CDR and no interpolation to be used. Oscilloscope must have a minimum bandwidth of 21GHz.



20 Measure differential amplitude voltage (V_0) for bits 57 to 62 using the equation:

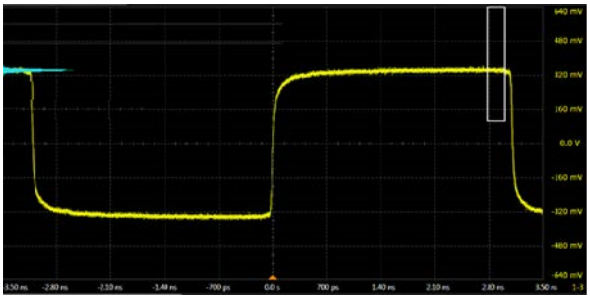
$$V_0 = [|V_{bits(57\text{-}62)} \text{ (64 bits of 1's)} - V_{bits(57\text{-}62)} \text{ (64 bits of 0's)}|]$$

21 Set the DUT to Preset 15 (P15).

22 Configure the DUT transmitter to output alternating square pattern of 64 0's and 64 1's on all lanes with SSC enabled but with both pre-shoot and de-emphasis disabled.

23 Adjust vertical scale such that the signal fits within the Oscilloscope's display

24 Average one cycle using 150 cycles; no CDR and no interpolation to be used. Oscilloscope must have a minimum bandwidth of 21GHz.



25 Measure differential amplitude voltage (V_{15}) for bits 57 to 62 using the equation:

$$V_{15} = [|V_{bits(57\text{-}62)} \text{ (64 bits of 1's)} - V_{bits(57\text{-}62)} \text{ (64 bits of 0's)}|]$$

Set Swing to be $20 * \log_{10} [V_0/V_{15}]$

26 Repeat the test for the remaining USB lanes.

Expected / Observable Results

If the Pre-Shoot for a particular Preset number is not within ± 1dB of the matching value in Table 13, the status of test is FAIL.

If the De-Emphasis for a particular Preset number is not within ± 1dB of the matching value in Table 13, the status of test is FAIL.

If Swing < 2.5 dB or Swing > 4.5 dB, the status of test is FAIL.

Test References

See

- Universal Serial Bus 4 (USB Type-C) Specification Version 1.00 (Table 3-5)
- Universal Serial Bus 4 (USB Type-C) Specification Version 1.00 (Table 5-5)

Tx Electrical Idle Voltage Test

NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of the Electrical Idle Voltage Test is to confirm that the transmitter peak voltage during electrical idle do not exceed the limits of the specification.

Test Pass Requirement

Tx Electrical Idle Voltage ≤ 20.00 mV_{p-p}

Test Setup

1 For the physical connection between the DUT & the Oscilloscope, see Figure 174 and for configuring the USB4 Test Application, see "Setting up the USB4 Test Application" on page 48.

2 Perform Channel Skew Calibration and configure settings for Preset Calibration. Refer to "Calibration Setup for Compliance Tests" on page 56.

3 Under the **Select Tests** tab of the USB4 Test Application, ensure that the required tests under the test group **Tx Electrical Idle Voltage** are selected.

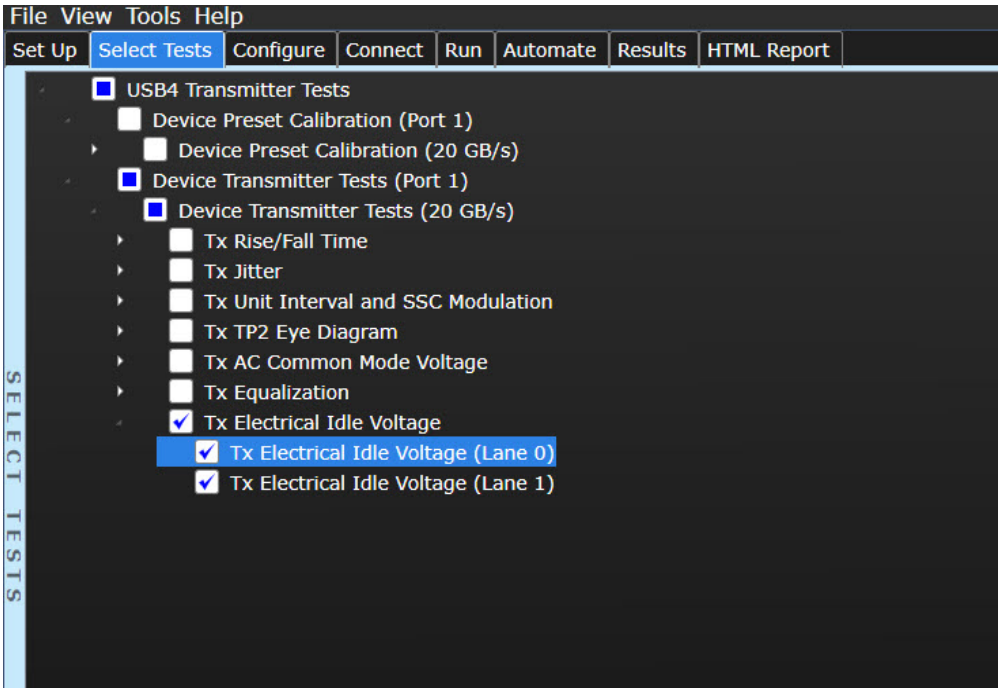


Figure 204 Selecting the Tx Electrical Idle Voltage Tests

Test Procedure

1 Configure the DUT to be in electrical idle mode.
2 Capture the waveform, and process it with the Digital Oscilloscope.
   a Sampling Rate ≥ 80 GSa/s.
   b Evaluate 10 Mpts per channel when using 80 GSa/s. For higher sampling rate, use memory depth in the same ratio to 10 Mpts.
   c No CDR, no average, and no interpolation to be used.
   d Oscilloscope must have a minimum bandwidth of 16 GHz (Gen 2) 21 GHz (Gen 3).
3 Calculate the TX Electrical Idle Voltage (V_ELEC_IDLE) using this equation:
   $V_{PEAK} = V_{TX-P} - V_{TX-N}$
4 $V_{\_ELEC\_IDLE}$ shall be extracted after applying first order low-pass filter with 3 dB point at 1.25 GHz.
5 Repeat the test for the remaining USB4 lanes.

Measurement Procedure

1 Verify the input signal.
   a Verify the input signal's amplitude.
   b Scale the vertical display of the input signal to optimum value.
2 Capture the input signal, and create the differential signal.
3 Setup the parameter of the general measurement.
   a Enable measure all edges to obtain the statistical values of the measurement.
4 Setup the following measurement:
   a Peak-to-peak voltage (V_{pp})
   b Root-mean-square voltage (V_{rms})
5 Report the Electrical Idle Output Voltage measurement results.

Expected / Observable Results

V_ELEC_IDLE > 20 mV_{p-p}, the status of test is FAIL

Test References

See

- *Universal Serial Bus 4 (USB Type-C) Specification Version 1.00 (Table 3-3)*

Tx Differential Return Loss Test

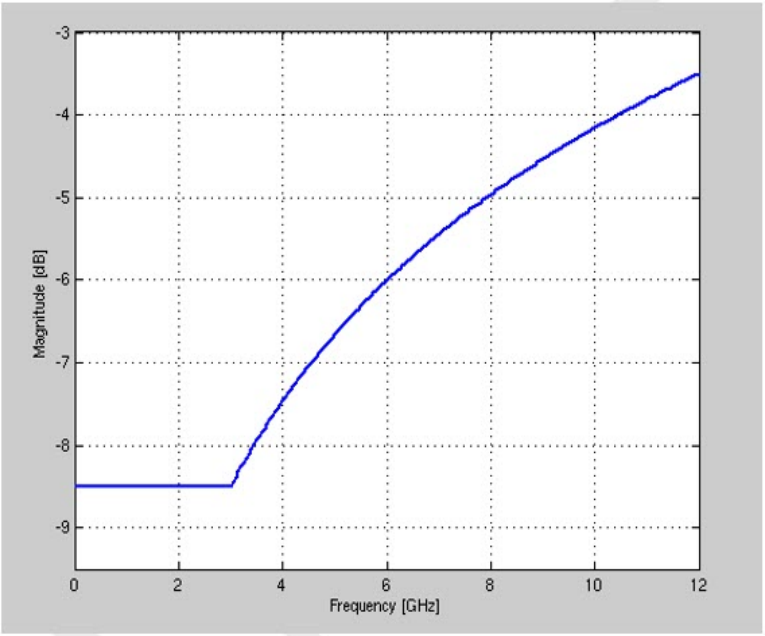
NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of this test is to confirm that the Differential Return Loss of a USB4 device is less than the maximum limit.

Test Pass Requirement

$$SDD11(f) = \begin{cases} -8.5 & 0.05 < f_{GHz} \leq 3 \\ -3.5 + 8.3 \cdot \log 10\left(\frac{f_{GHz}}{12}\right) & 3 < f_{GHz} \leq 12 \end{cases}$$



Test Setup

1 For the physical connections between the DUT & the Oscilloscope, see the connection diagrams in Figure 205 and Figure 206.

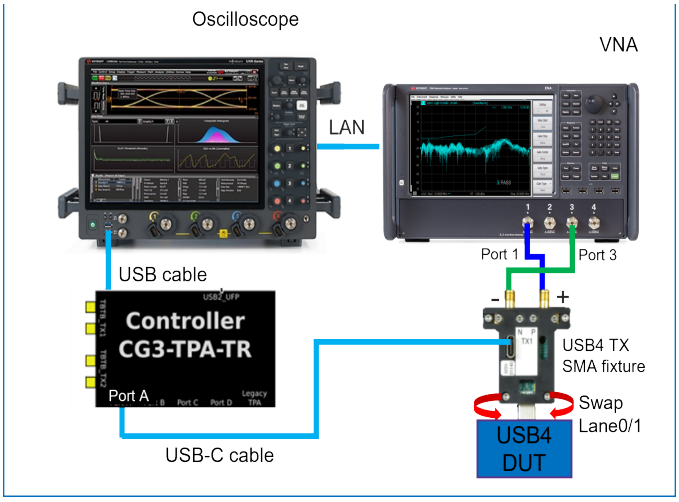


Figure 205 Tx Return loss test setup with Tx SMA test fixture

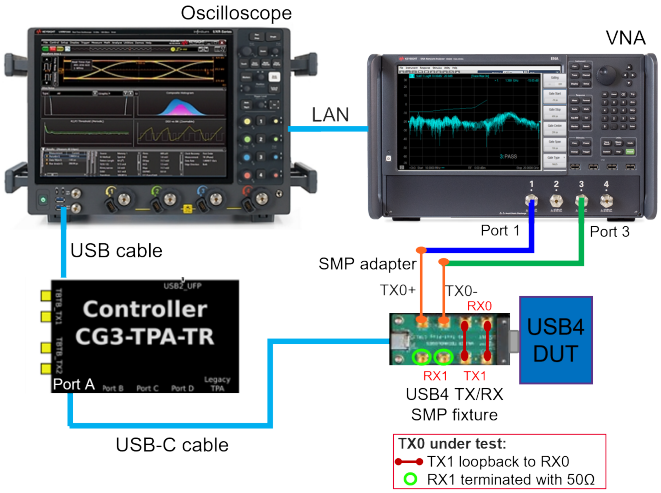
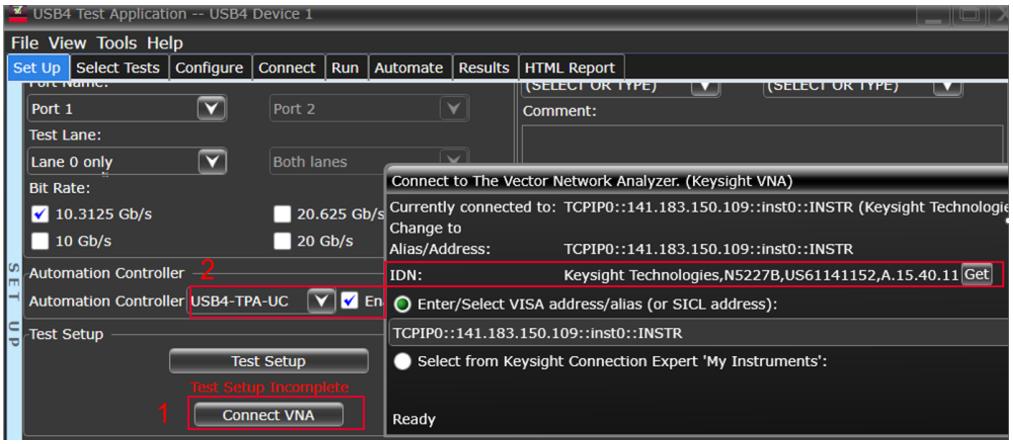


Figure 206 Return loss test setup with Tx/Rx SMP test fixture

2 In the **Set Up** tab, please connect VNA in the Tx app.

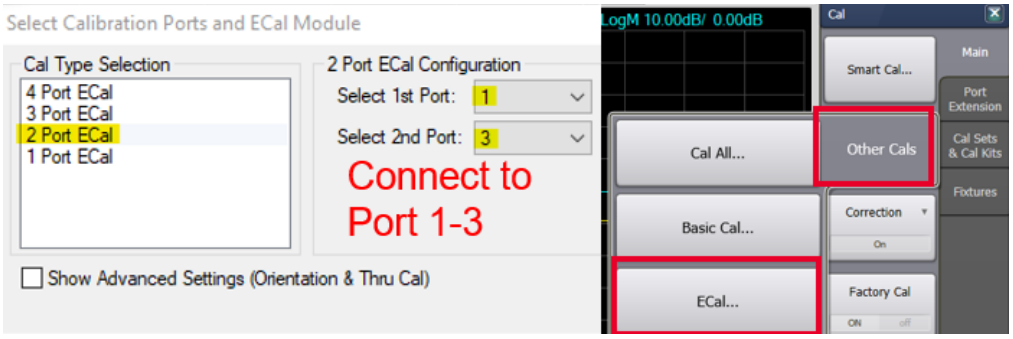


3 Prior calibration, setup Network Analyzer with following sweep settings:

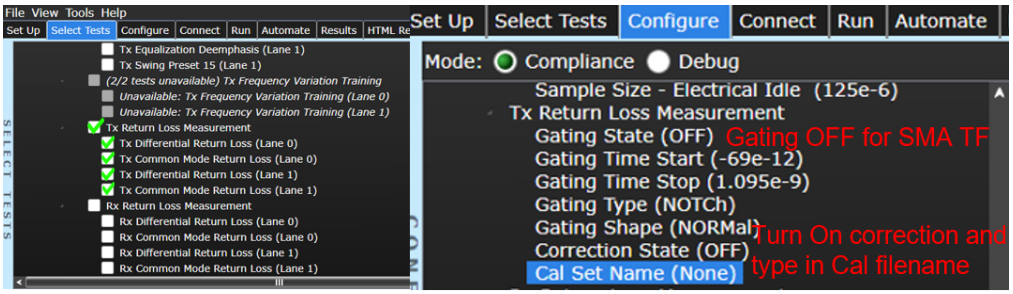
- Frequency range of 10 MHz to 12 GHz
- IF BW of 1 kHz
- At least 1600 points
- Impedance 85 ohm differential
- Define the Topology to Bal using VNA Port 1 and Port 3

NOTE Ensure that the VNA firmware revision is A.17.25.05 or higher to be compatible with the return loss test automation.

4 Run calibration on the network analyzer and test cables using a 2-port electronic kit (ECal). Save the Cal file.



5 In the **Select** test tab, select the Tx Return Loss Measurement and set the parameters in the **Configure** tab as shown in the figure below.



NOTE Please note that no gating setup is required for SMA fixture.

6 The test application sets USB4ETT **Tool Usage Mode**, commands VNA to measure Tx Return Loss in S2P, and compiles result using SigTest.

7 In the test setup, please flip the Tx fixture to swap the test lanes 0 and 1.

8 In case of SMP test fixture, Tx/Rx lane under test can be switched as shown in Figure 207.

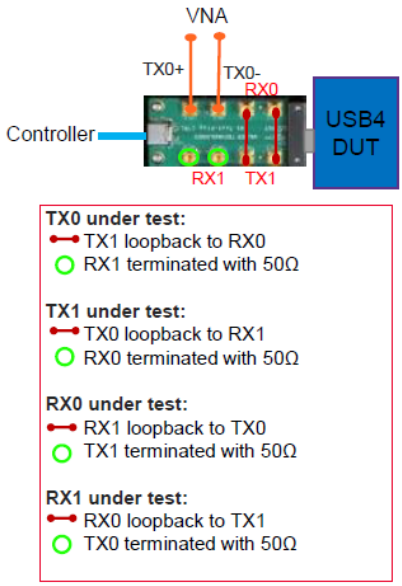


Figure 207 SMP test fixture - Tx/Rx lane switching

Test Procedure

1 Choose a supported USB4 speed to start with.
2 The test application sets USB4ETT tool to configure the DUT transmitter to output PRBS31 on all lanes with SSC turned on.
3 Connect Lane under test TX_P, TX_N to the Network Analyzer.
4 Measure the Differential R. Loss with the Network Analyzer and compile the result using SigTest.
5 If Differential Return loss violates the above requirement, then the result is Fail.
6 Repeat the test for all remaining USB4 lanes.
7 Repeat the test for all supported USB4 Gen2 and Gen3 speeds.

Expected / Observable Results

If Differential Return Loss violated the specified requirement, then Fail.

Test References

See

- *USB4 Specification Version 2.00, Table 3-2*

Tx Common Mode Return Loss Test

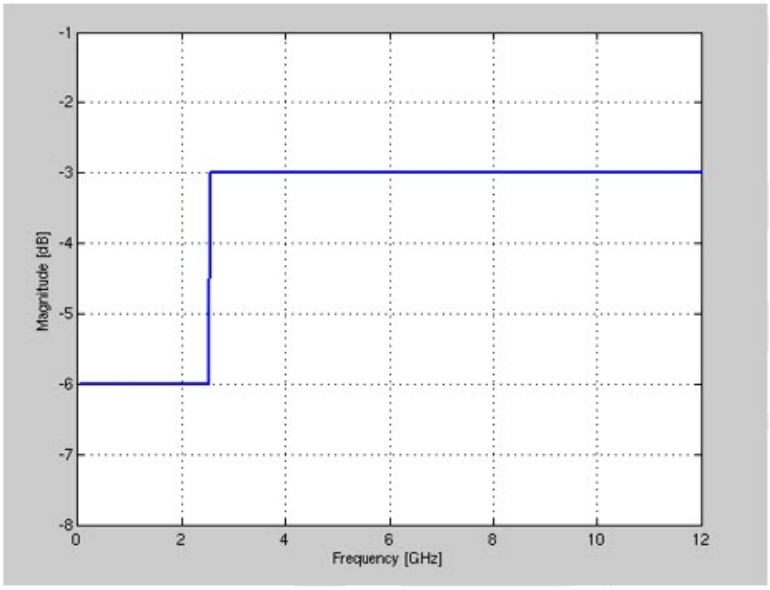
NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of this test is to confirm that the Common Mode Return Loss of a USB4 device is less than the maximum limit.

Test Pass Requirement

$$SCC11(f) = \begin{cases} -6 & 0.05 < f_{GHz} \leq 2.5 \\ -3 & 2.5 < f_{GHz} \leq 12 \end{cases}$$



Test Setup

1 For the physical connections between the DUT & the Oscilloscope, see the connection diagrams in Figure 208 and Figure 209.

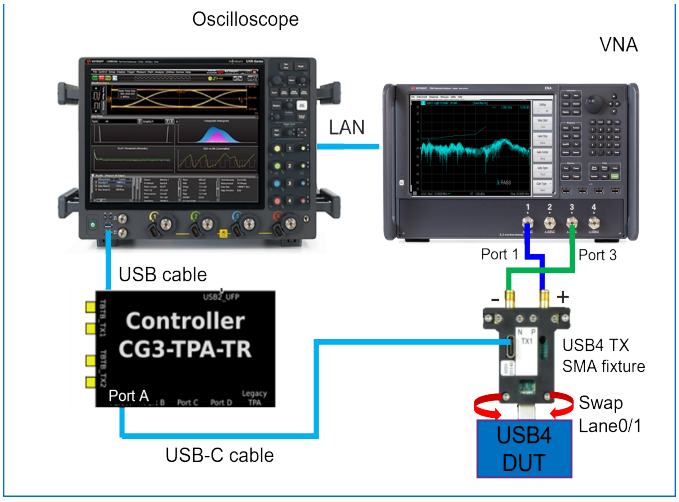


Figure 208 Tx Return loss test setup with Tx SMA test fixture

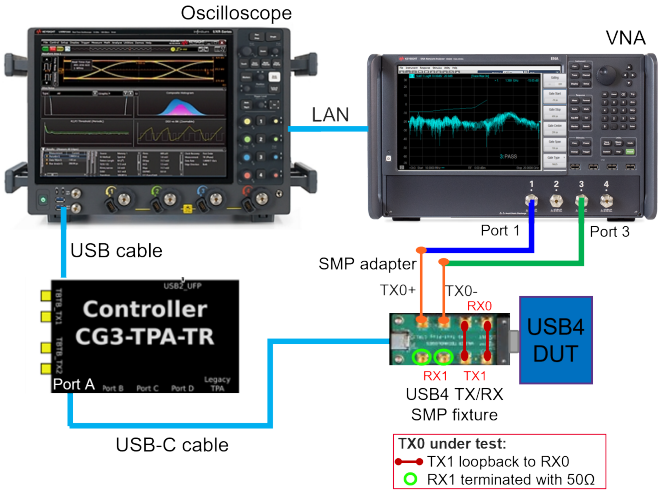
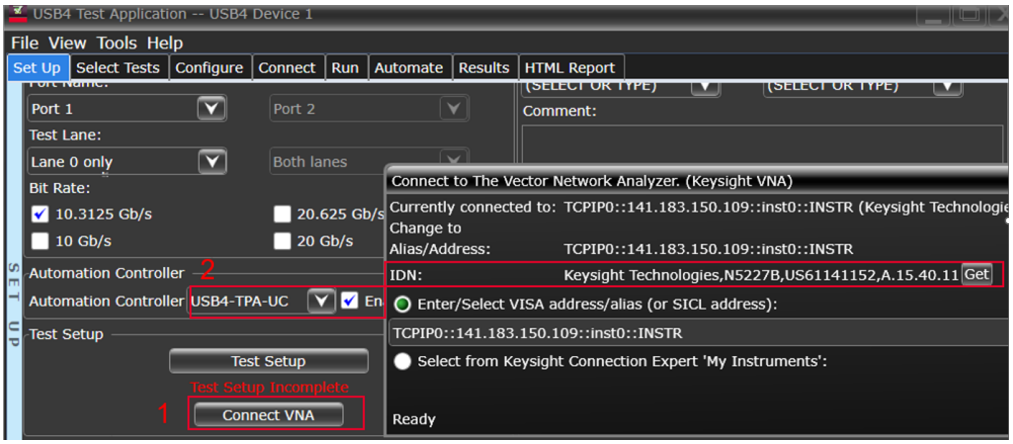


Figure 209 Return loss test setup with Tx/Rx SMP test fixture

2 In the **Set Up** tab, please connect VNA in the Tx app.

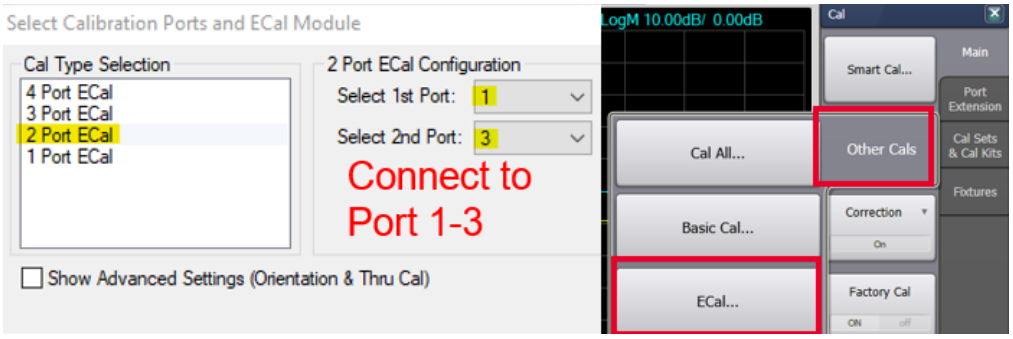


3 Prior calibration, setup Network Analyzer with following sweep settings:

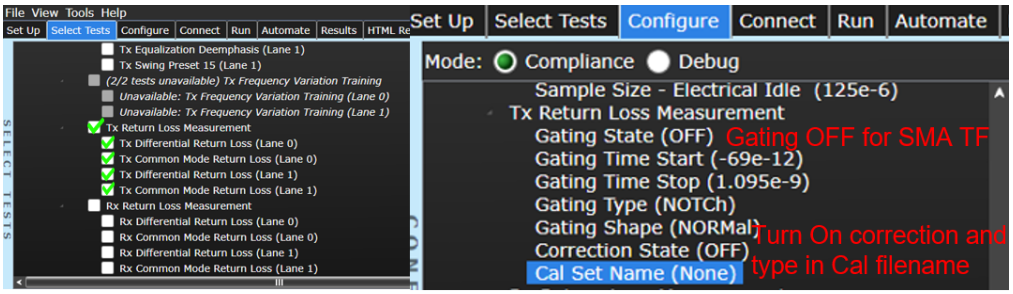
- Frequency range of 10 MHz to 12 GHz
- IF BW of 1 kHz
- At least 1600 points
- Impedance 85 ohm differential
- Define the Topology to Bal using VNA Port 1 and Port 3

NOTE Ensure that the VNA firmware revision is A.17.25.05 or higher to be compatible with the return loss test automation.

4 Run calibration on the network analyzer and test cables using a 2-port electronic kit (ECal). Save the Cal file.



5 In the **Select** test tab, select the Tx Return Loss test and set the parameters in the **Configure** tab as shown in the figure below.



NOTE Please note that no gating setup is required for SMA fixture.

6 The test application sets USB4ETT **Tool Usage Mode**, commands VNA to measure Tx Return Loss in S2P, and compiles result using SigTest.

7 In the test setup, please flip the Tx fixture to swap the test lanes 0 and 1.

8 In case of SMP test fixture, Tx/Rx lane under test can be switched as shown in Figure 210.

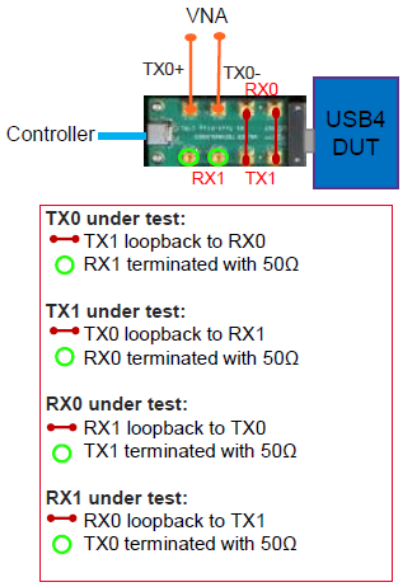


Figure 210 SMP test fixture - Tx/Rx lane switching

Test Procedure

1 Choose a supported USB4 speed to start with.
2 The test application sets USB4ETT tool to configure the DUT transmitter to output PRBS31 on all lanes with SSC turned on.
3 Connect Lane under test TX_P, TX_N to the Network Analyzer.
4 Measure the Common Mode Return Loss with the Network Analyzer and compile the result using SigTest.
5 If Common Mode Return loss violates the above requirement, then the result is Fail.
6 Repeat the test for all remaining USB4 lanes.
7 Repeat the test for all supported USB4 Gen2 and Gen3 speeds.

Expected / Observable Results

If Common Mode Return Loss violated the specified requirement, then Fail.

Test References

See

- *USB4 Specification Version 2.00, Table 3-2*

Rx Differential Return Loss Test

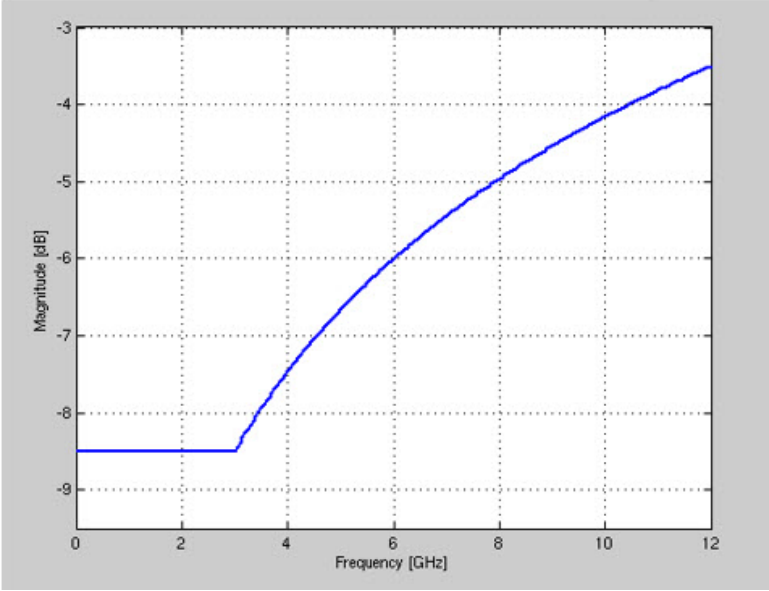
NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of this test is to confirm that the Differential Return Loss of a USB4 device is less than the maximum limit.

Test Pass Requirement

$$\text{SDD22(f)} = \begin{cases} -8.5 & 0.05 < f_{GHz} \leq 3 \\ -3.5 + 8.3 \cdot \log 10\left(\frac{f_{GHz}}{12}\right) & 3 < f_{GHz} \leq 12 \end{cases}$$



Test Setup

1 For the physical connections between the DUT & the Oscilloscope, see the connection diagrams in Figure 211 and Figure 212.

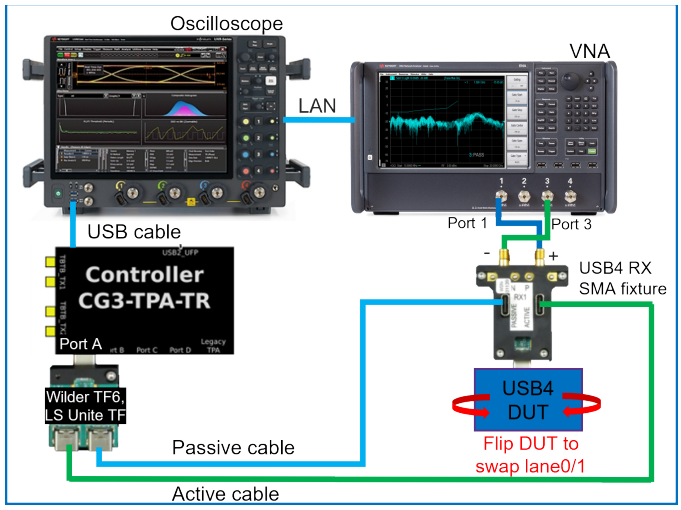


Figure 211 Tx Return loss test setup with Rx SMA test fixture

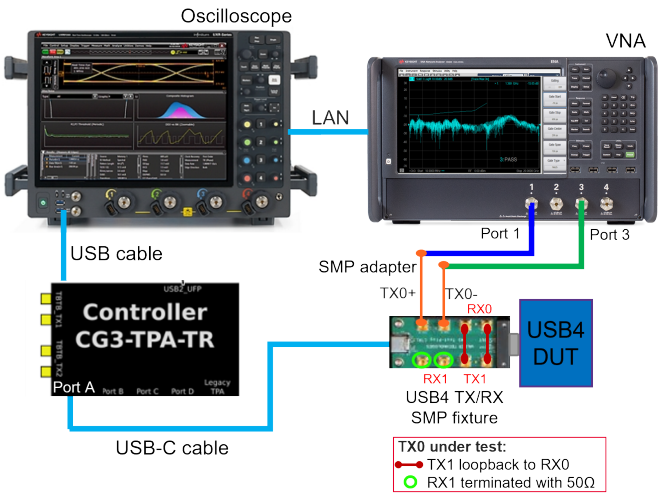
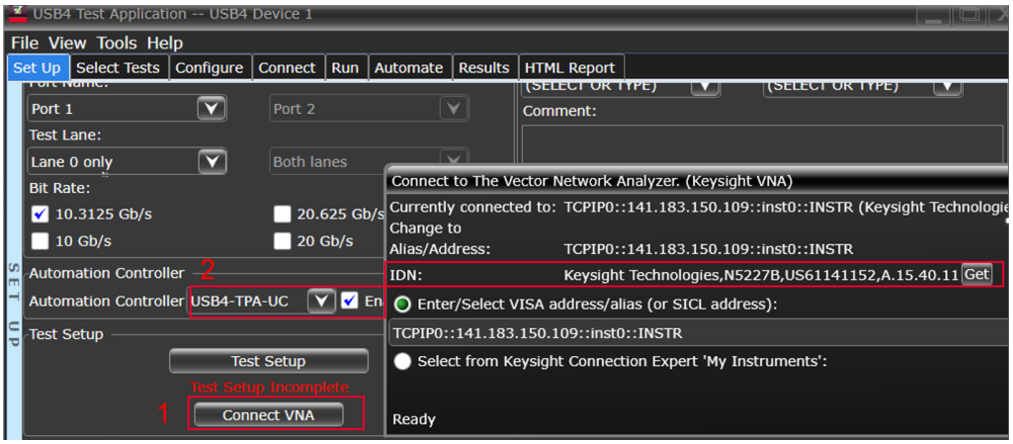


Figure 212 Return loss test setup with Tx/Rx SMP test fixture

2 In the **Set Up** tab, please connect VNA in the Tx app.

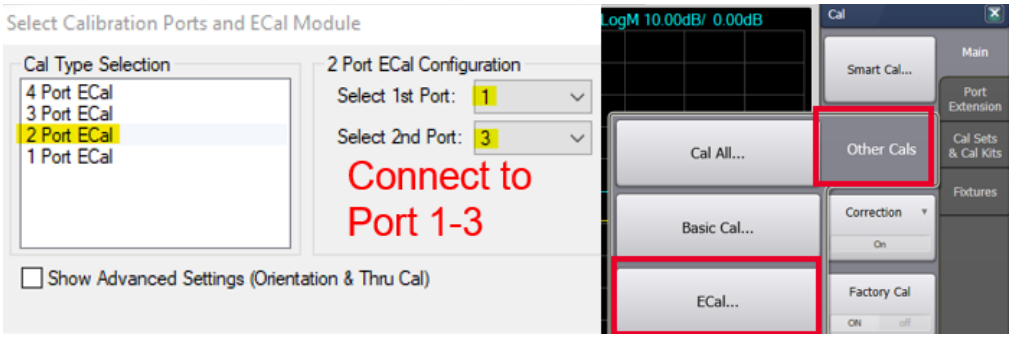


3 Prior calibration, setup Network Analyzer with following sweep settings:

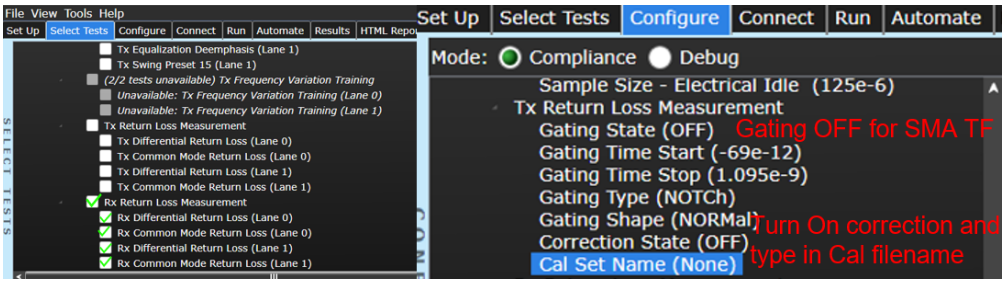
- Frequency range of 10 MHz to 12 GHz
- IF BW of 1 kHz
- At least 1600 points
- Impedance 85 ohm differential
- Define the Topology to Bal using VNA Port 1 and Port 3

NOTE Ensure that the VNA firmware revision is A.17.25.05 or higher to be compatible with the return loss test automation.

4 Run calibration on the network analyzer and test cables using a 2-port electronic kit (ECal). Save the Cal file.



5 In the **Select** test tab, select the Tx Return Loss test and set the parameters in the **Configure** tab as shown in the figure below.



NOTE Please note that no gating setup is required for SMA fixture.

6 The test application sets USB4ETT **Tool Usage Mode,** commands VNA to measure Tx Return Loss in S2P, and compiles result using SigTest.

7 In the test setup, please flip the Rx fixture to swap the test lanes 0 and 1.

8 In case of SMP test fixture, Tx/Rx lane under test can be switched as shown in Figure 213.

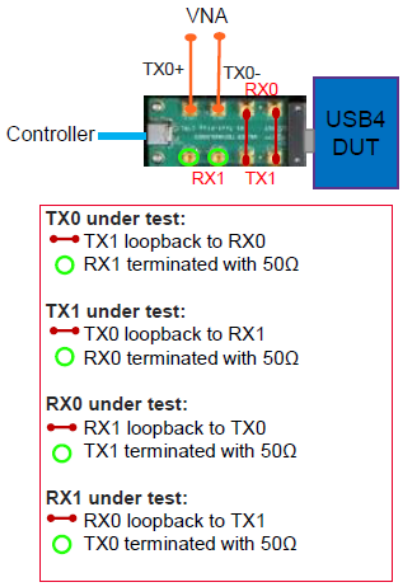


Figure 213 SMP test fixture - Tx/Rx lane switching

Test Procedure

1 Choose a supported USB4 speed to start with.
2 The test application sets USB4ETT tool to configure the DUT transmitter to output PRBS31 on all lanes with SSC turned on.
3 Connect a USB Type-C Passive cable from the Passive receptacle connector over the test fixture to the Low speed united coupon Passive receptacle connector that is connected to the USB4 Micro-controller PA.
4 Connect a USB Type-C Active cable from the Active receptacle connector over the test fixture to the Low speed united coupon Active receptacle connector that is connected to the USB4 Micro-controller PA.
5 Connect Lane under test RX_P, RX_N to the Network Analyzer.
6 Measure the Differential R. Loss with the Network Analyzer and compile the result using SigTest.
7 If Differential Return loss violates the above requirement, then the result is Fail.
8 Repeat the test for all remaining USB4 lanes.
9 Repeat the test for all supported USB4 Gen2 and Gen3 speeds.

Expected / Observable Results

If Differential Return Loss violated the specified requirement, then Fail.

Test References

See

- *USB4 Specification Version 2.00, Table 3-9*

Rx Common Mode Return Loss Test

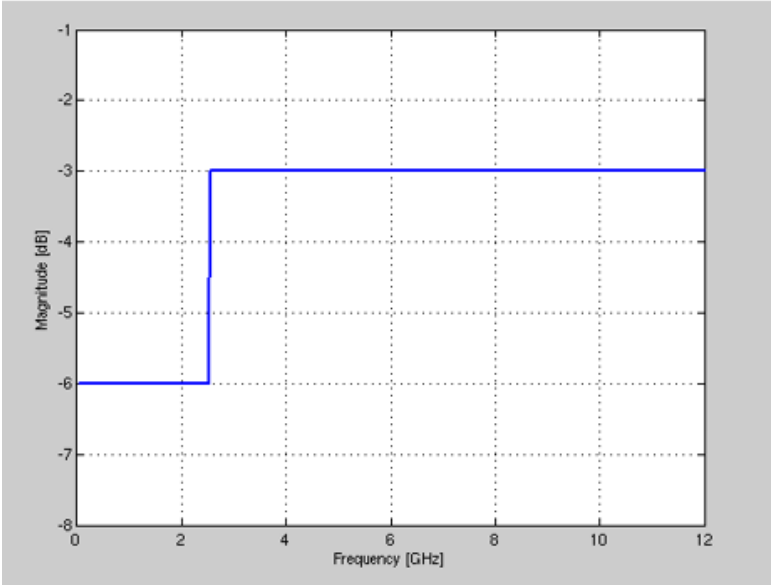
NOTE When running the Test App on a 2-Channel Oscilloscope, the **Select Tests** tab shall display tests pertaining to either **Lane 0 only** or to **Lane 1 only**.

Test Overview

The objective of this test is to confirm that the Common Mode Return Loss of a USB4 device is less than the maximum limit.

Test Pass Requirement

$$SCC22(f) = \begin{cases} -6 & 0.05 < f_{GHz} \leq 2.5 \\ -3 & 2.5 < f_{GHz} \leq 12 \end{cases}$$



Test Setup

1 For the physical connections between the DUT & the Oscilloscope, see the connection diagrams in Figure 214 and Figure 215.

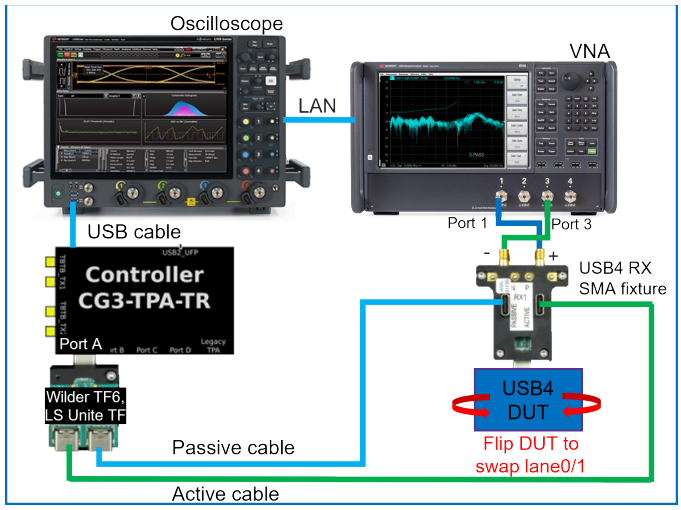


Figure 214 Tx Return loss test setup with Rx SMA test fixture

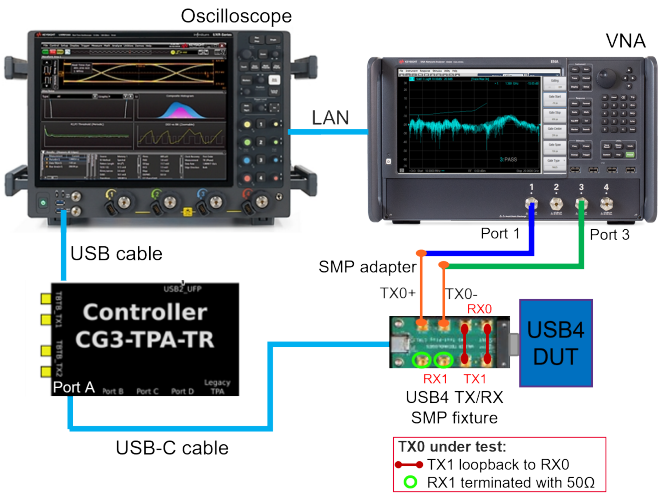
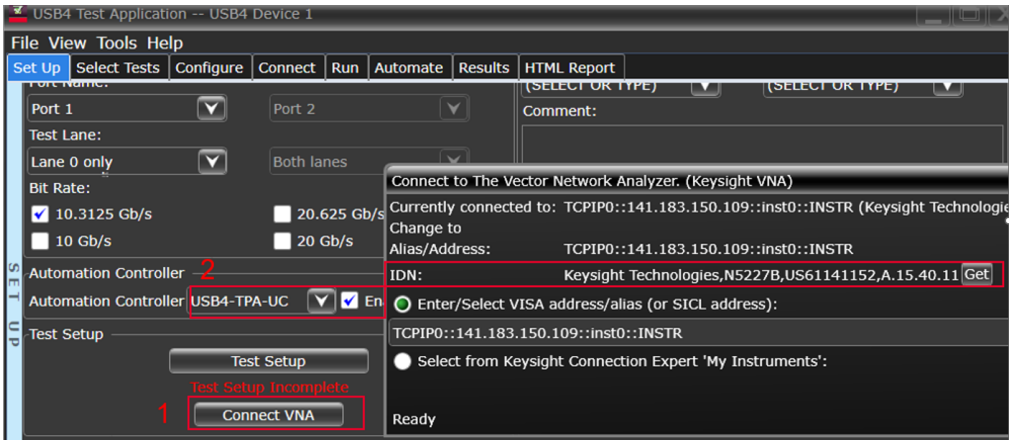


Figure 215 Return loss test setup with Tx/Rx SMP test fixture

2 In the **Set Up** tab, please connect VNA in the Tx app.

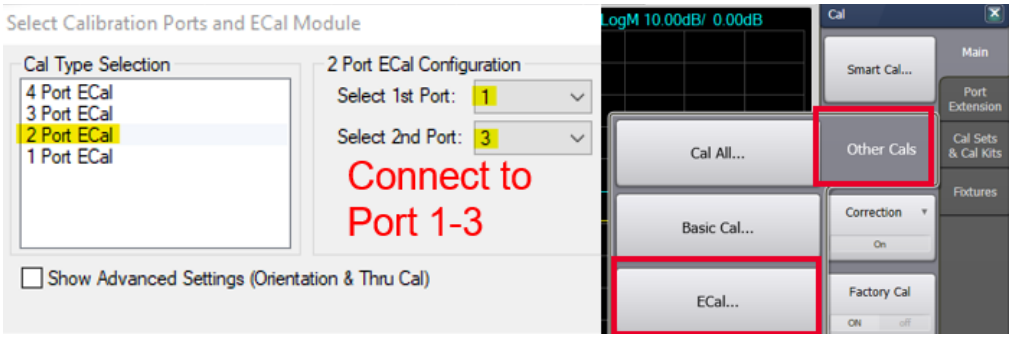


3 Prior calibration, setup Network Analyzer with following sweep settings:

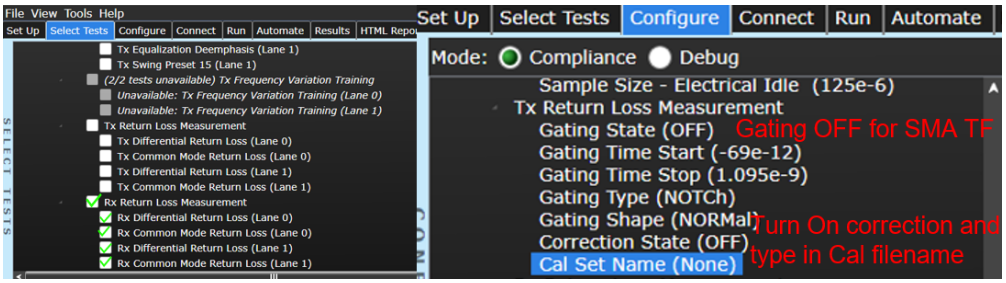
- Frequency range of 10 MHz to 12 GHz
- IF BW of 1 kHz
- At least 1600 points
- Impedance 85 ohm differential
- Define the Topology to Bal using VNA Port 1 and Port 3

NOTE Ensure that the VNA firmware revision is A.17.25.05 or higher to be compatible with the return loss test automation.

4 Run calibration on the network analyzer and test cables using a 2-port electronic kit (ECal). Save the Cal file.



5 In the **Select** test tab, select the Tx Return Loss test and set the parameters in the **Configure** tab as shown in the figure below.



NOTE Please note that no gating setup is required for SMA fixture.

6 The test application sets USB4ETT **Tool Usage Mode,** commands VNA to measure Tx Return Loss in S2P, and compiles result using SigTest.

7 In the test setup, please flip the Rx fixture to swap the test lanes 0 and 1.

8 In case of SMP test fixture, Tx/Rx lane under test can be switched as shown in Figure 216.

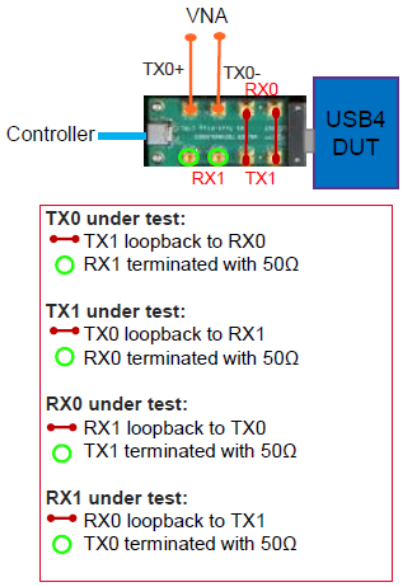


Figure 216 SMP test fixture - Tx/Rx lane switching

Test Procedure

1 Choose a supported USB4 speed to start with.
2 The test application sets USB4ETT tool to configure the DUT transmitter to output PRBS31 on all lanes with SSC turned on.
3 Connect a USB Type-C Passive cable from the Passive receptacle connector over the test fixture to the Low speed united coupon Passive receptacle connector that is connected to the USB4 Micro-controller.
4 Connect a USB Type-C Active cable from the Active receptacle connector over the test fixture to the Low speed united coupon Active receptacle connector that is connected to the USB4 Micro-controller.
5 Connect Lane under test RX_P, RX_N to the Network Analyzer.
6 Measure the Common Mode Return Loss with the Network Analyzer and compile the result using SigTest.
7 If Common Mode Return loss violates the above requirement, then the result is Fail.
8 Repeat the test for all remaining USB4 lanes.
9 Repeat the test for all supported USB4 Gen2 and Gen3 speeds.

Expected / Observable Results

If Common Mode Return Loss violated the specified requirement, then Fail.

Test References

See

USB4 Specification Version 2.00, Table 3-9

Index

A

application software, installing, 38
application software, starting, 45
Automation tab, 47

C

calibrating the oscilloscope, 44

E

Equation
  AC Common Mode Voltage, 147, 232, 317, 401
  De-Emphasis, 152, 236, 321, 405
  differential amplitude voltage, 151, 235, 320, 404
  Pre-Shoot, 152, 236, 321, 405
  SSC Deviation percentage, 138, 224, 308, 392
  Swing, 153, 237, 322, 406
  Total Jitter, 120, 126, 208, 214, 292, 298, 376, 382
  Uncorrelated Jitter, 110, 198, 282, 366
  Uncorrelated Jitter TP3EQ, 122, 210, 294

I

installation, 29, 37

L

license key, installing, 39
Low insertion loss phase matched cables, 32

M

measurements, preparing, 43
mouse, 31

O

Online Help, 36
oscilloscope calibration, 44

R

Real Time Scopes, 32
Results tab, 47
Run Tests tab, 47

T

Test Point Access Boards, 31
Thunderbolt standard specifications, 36