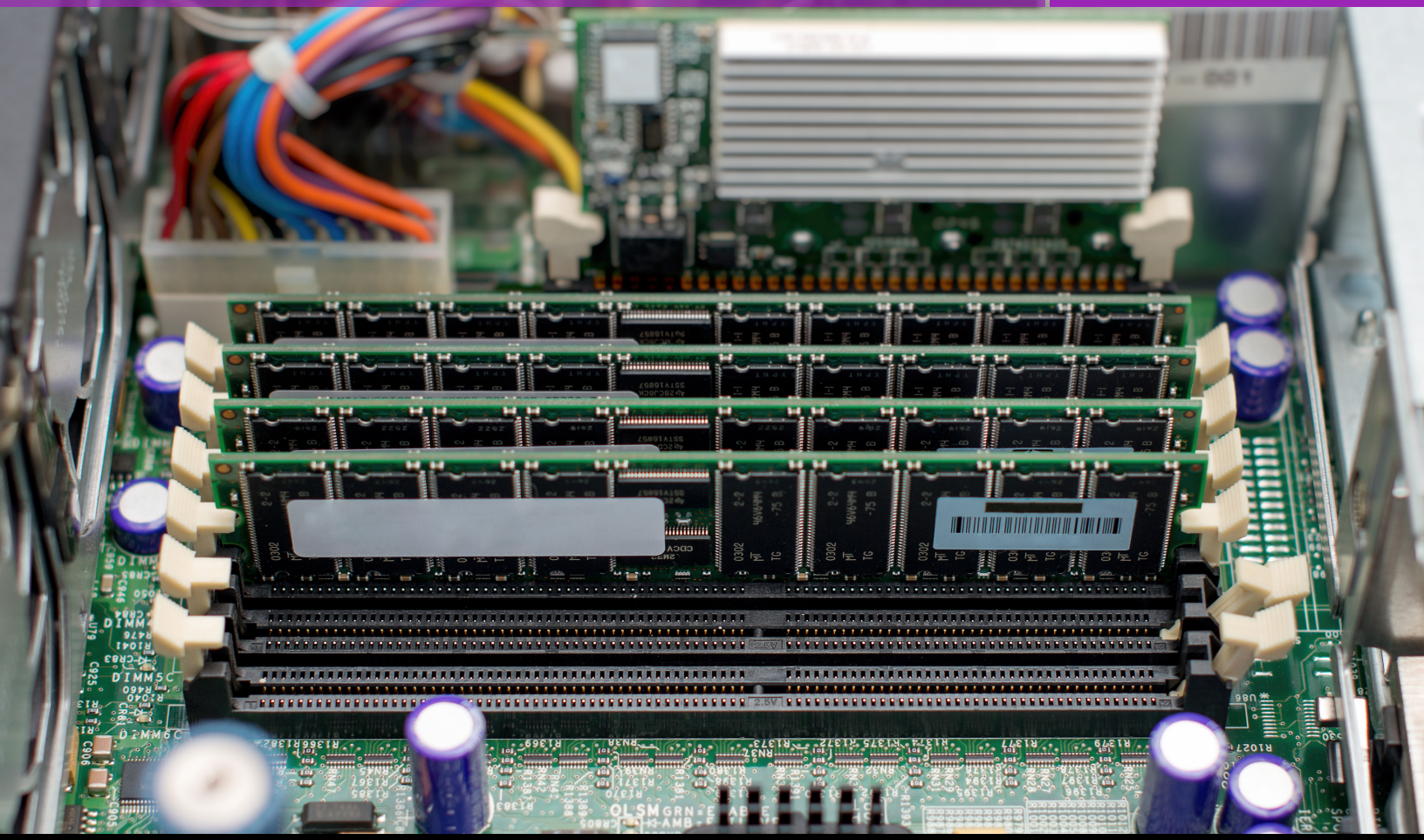
WHITE PAPER



DDR Memory

Test Challenges from DDR3 to DDR5

KEYSIGHT

DDR Overview

Cloud, networking, enterprise, high-performance computing, big data, and artificial intelligence are propelling the development of double data rate (DDR) memory chip technology. Demand for lower power requirements, higher density for more memory storage, and faster transfer speeds are constant. Servers drive the demand for next-generation DDR. Consumers benefit when existing and legacy generations economize and become affordable. As dynamic random-access memory (DRAM) decreases in price, it makes its way into our PCs and laptops.

To accommodate these requirements, standardization body JEDEC (Joint Electron Device Engineering Council) released the DDR5 synchronous dynamic random-access memory (SDRAM) standard in July 2020. Starting in mid-2021, JEDEC expects to start seeing DDR5 devices emerge as manufacturers confirm hardware.

The Benefits of DDR5 over DDR4

DDR5 offers a number of benefits over the previous generation, including the following:

- faster transfer speeds
- increased efficiency
- improved data integrity
- more memory

Although it's still in the early adoption phase, DDR5 will double the bandwidth in each dual in-line memory module (DIMM) over DDR4. DDR4 bandwidth ranges from 1,600 million transfers per second (MT/s) to a more recently attained 3,200 MT/s. DDR5 increases memory density and doubles DDR4's throughput frequency to a potential maximum of 6,400 MT/s. If you are more comfortable dealing with gigabits per second (Gbps), DDR4's data transfer rate ranges from 1.6 to 3.2 Gbps. DDR5 supports data transfer rates from 4.8 to 6.4 Gbps.

DDR5 supports a higher input / output speed. Its burst length of 16 is twice that of DDR4. A DDR5 DIMM has two independent subchannels that support the same data width as DDR4. The independent subchannels improve memory controller scheduling and support concurrent operations.

DDR5 is about improving density more than speed. It is meant to be stackable to eight chips high, increasing capacity, and it supports 32 banks in eight bank groups. DDR5's same-bank refresh function enables a CPU core to use other DDR5 banks if one is already in use. The technology integrates error-correcting code (ECC) in-chip. (ECC finds and corrects errors before it sends data to the CPU.) DDR5 supports normal ECC.

DDR5 lowers operating voltage by a small amount. Its modules will run at 1.1 V, compared with 1.2 V on DDR4. A lower operating voltage means better power efficiency. As the internet infrastructure continues to grow and DIMMs proliferate, a little bit of power saved in each DIMM adds up. Thus, JEDEC has reduced the thermal load in data centers. DDR5 modules will feature voltage regulators integrated onto each stick, or DIMM, which takes responsibility for managing power from the motherboard.

It seems as though DDR5 improves everything, except for a small inconvenience in design and manufacturing. A DDR5 SDRAM DIMM is not a drop-in replacement. Although both DDR4 and DDR5 modules have 288 pins, the pins do not share the same layout. The DDR5 DIMM will need a new slot. However, like DDR4, DDR5 still uses a ball grid array (BGA) package and has the x4/x8 common footprint.

DDR5 enables server workloads to more than double in performance while slightly reducing power consumption — both great benefits to data centers worldwide.

DDR5 Doubles the Data Rate

DDR5 delivers twice the performance and much-improved power efficiency. It provides more than 6 GT/s and a terabit of memory, which offers the following:

- faster transfer speed
- increased efficiency
- more memory

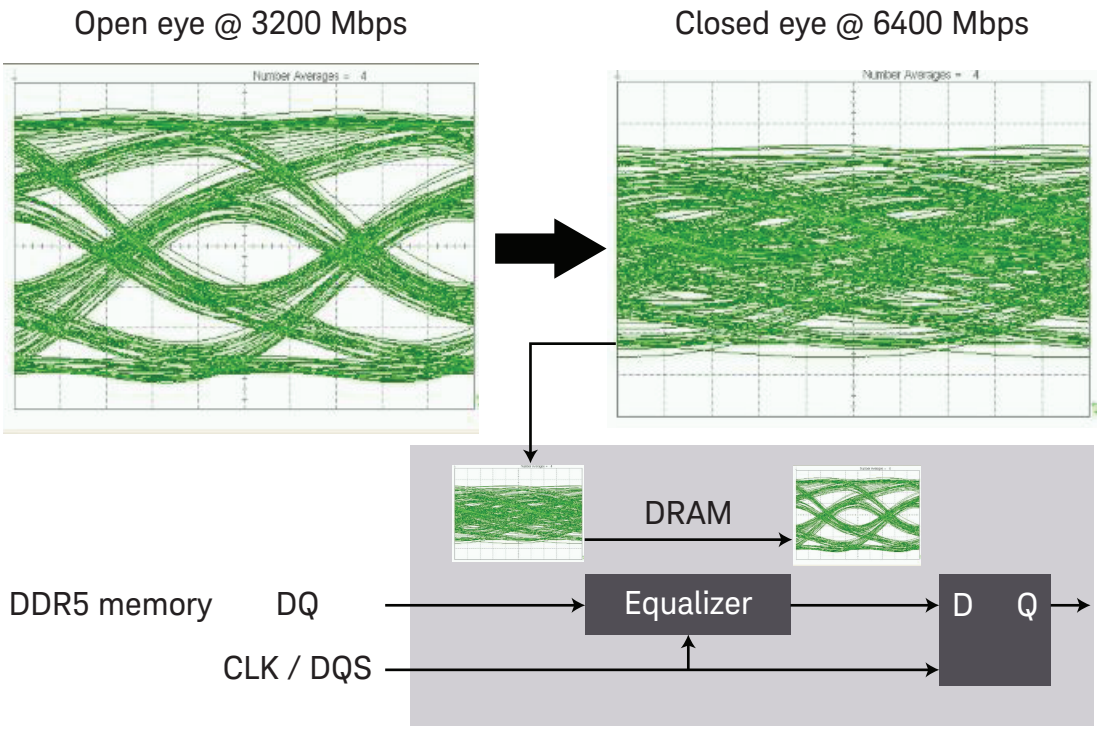


Figure 1. Twice as fast as DDR4 memory, DDR5 memory is more complex in nearly every area. The eyes close further and require equalization in transmission.

Test Challenges

Signal integrity and data corruption issues can make testing DDR designs problematic. Understanding the issues is the first step toward solving them.

Signal integrity

A common signal integrity challenge found in DDR designs is timing issues with the memory controller. It is likely you purchased the memory controller with your design rather than designing a custom memory controller. If so, you will need to adjust the timing between your board and memory controller. Historically, it was enough to run setup and hold time tests to verify data transfer. In the past, speeds were slower, so margins were wider, meaning you had enough room to declare a DDR2 or DDR3 design within specification as long as you passed a setup and hold time test.

However, with faster speed comes tighter margins. If you are working with DDR4 or DDR5, you no longer have enough margin to pass specifications with simple setup and hold time testing. Verifying DDR4 or DDR5 requires an eye diagram.

The DDR4 standard requires a specific margin and tolerances for random jitter and bit error rate within the specification. From this standard, you can create a mask in your oscilloscope. A mask defines a region on the oscilloscope's display in which the waveform must remain to meet the requirements of your standard. If the eye closes too much and enters the mask, you likely have bit errors and will fail specification.

DDR5 eyes start closing at the solder balls of the DRAM package around 4 GT/s (or 4,000 MT/s), depending on the signal integrity of the system under test (or device under test). The DDR5 specification is defined at the solder balls of the DRAM because probing inside the chip package is exceptionally difficult when in-system. Unfortunately, probing at the solder balls of the DRAM does not tell you if the eye is open or closed in the chip. Therefore, you must compensate with a decision feedback equalizer (DFE). A four-tap DFE, as described in the DDR5 specification, is necessary to remove the impulse response effects of the channel.

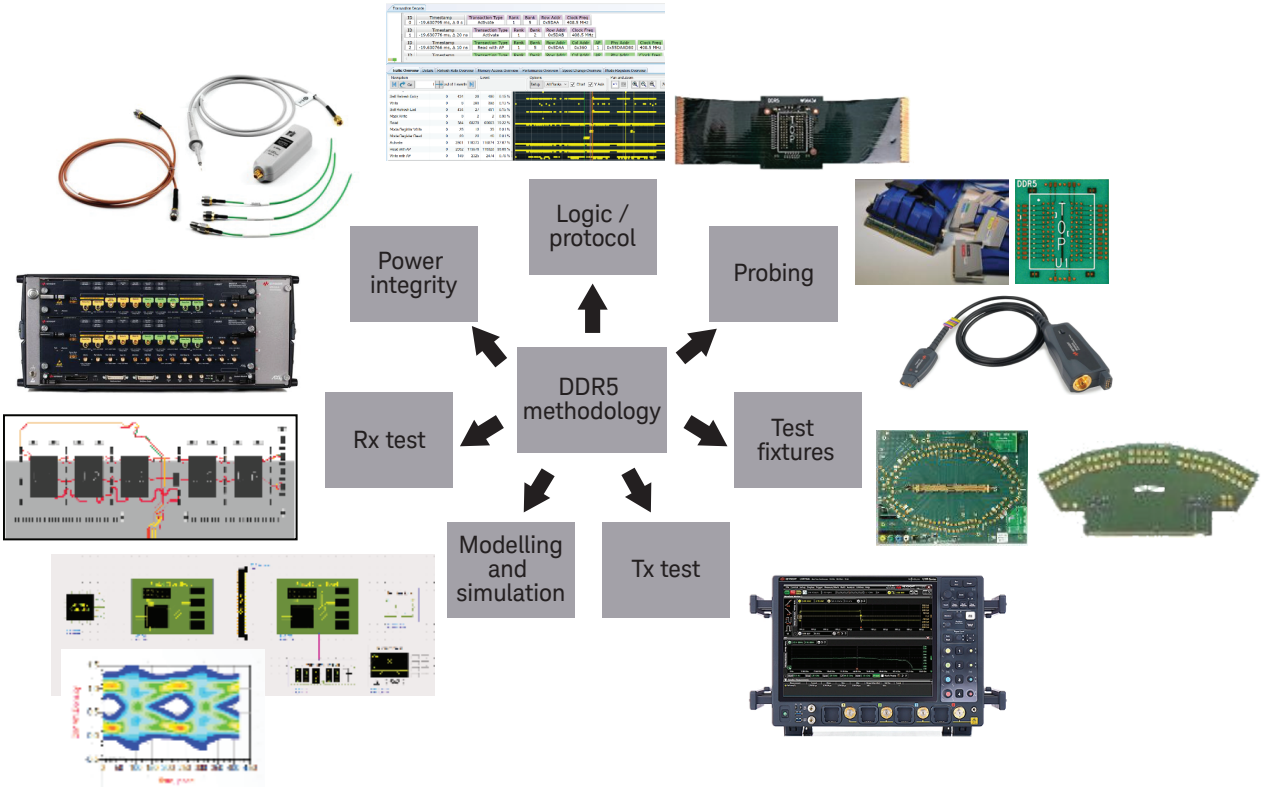


Figure 2. Developing with DDR5 is easier with a complete ecosystem of design, measurement, and test solutions that work well with each other.

Data corruption

When validating a DDR4, LPDDR4, DDR5, or LPDDR5 design, you may encounter data corruption issues. Data corruption has a broad range of causes, typically signal integrity and functional issues. Oscilloscopes validate and debug the integrity of the signals (including eye size, rise and fall times, and power integrity), while logic analyzers debug and validate the functional or protocol compliance of memory systems.

Functional issues, where the memory devices do not receive the correct commands in the proper sequence or within specified timings, can result in data corruption and system crashes. Testing is essential to identify these errors and their causes, whether physical or functional, so you can debug your design and prevent failures.

Test Equipment Alleviates the Challenges

You can use compliance test software to make testing and debugging easier.

Compliance test software runs on your oscilloscope to help validate the signal integrity and physical layer of your design. It automates the compliance test, verifies your design results, and generates a pass / fail report. All you need to do is connect the signals to your oscilloscope and run the application.

To test your design's functional or protocol compliance, the right logic analyzer can capture all DDR signals simultaneously (over 100 signals in DIMM / SODIMM / DRAM designs) at data rates up to 4,000 MT/s with trace depths of up to 400M samples per signal. For DDR5, protocol capture is possible with a logic analyzer at data rates up to 8,000 MT/s (when the column/address (CA) signals are operating at 4 GHz). Powerful analysis software decodes the memory protocol transactions and provides multiple views and graphs of the traffic flowing through the system. The views and graphs help validation engineers rapidly navigate the traffic flow to identify areas of concern. Protocol compliance validation software identifies exact issues in memory systems.

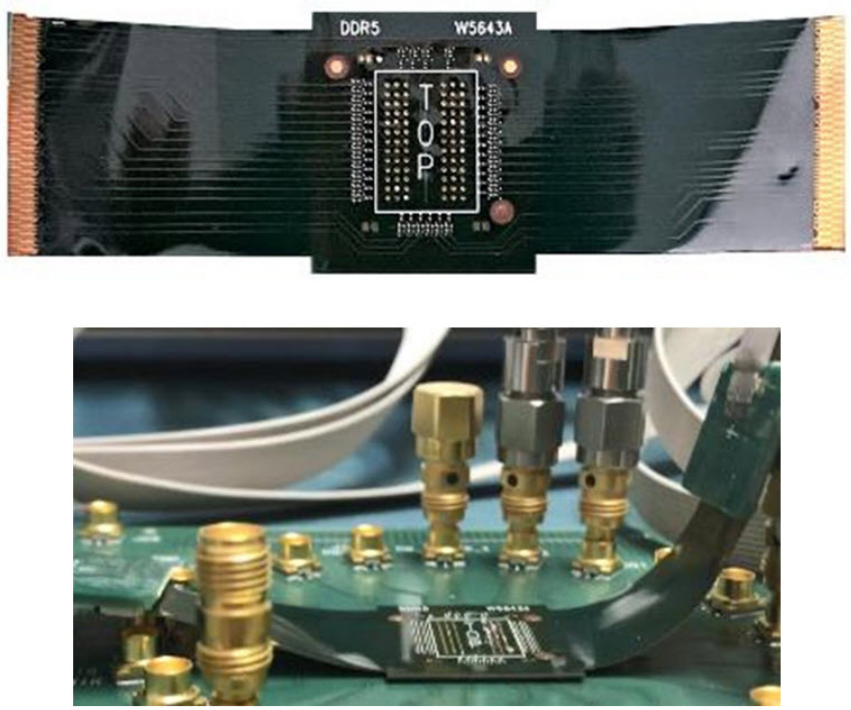


Figure 3. The DDR5 specification is defined at the solder balls of the DRAM because probing inside the chip package is exceptionally difficult when in-system.

Conclusion

DDR is a memory chip technology that has progressed through three generations in the past 13 years. Each generation has improved in speed, efficiency, and memory capacity. But as the standard allows for more data transferred at faster rates, margins decrease. Therefore, design work and testing become more challenging.

Oscilloscopes and compliance software can alleviate some of the challenges if you are working on the physical layer. Logic analyzers can help you test and debug your designs if you are working on functional and protocol compliance.

Learn More

Below is a list of recommended test equipment and software to test DDR.

DDR5

- UXR-Series oscilloscopes (16 GHz or more)
- D9050DDRC DDR5 Tx Compliance Test Software
- MX0023A InfiniiMax 25 GHz RC probe amp with MX0106A (23 GHz) InfiniiMax differential solder-in head and MX0105A (20 GHz) InfiniiMax differential SMA probe head
- U4164A logic analyzer system with U4164A-02G speed upgrade
- Logic analyzer software B4661A, B4661A-5FP / 5TP / 5NP
- M80885RCA DDR5 Receiver Conformance and Characterization Software

DDR4

- UXR-Series oscilloscopes (8 GHz or more)
- D9040DDRC DDR4 Compliance Test Application for Infiniium Series oscilloscopes
- U4164A logic analyzer system with U4164A-02G speed upgrade
- Logic analyzer software B4661A, B4661A-1FP / 1TP / 1NP, B4661A-3FP / 3TP / 3NP, B4661A-4FP / 4TP / 4NP

DDR3

- V-Series oscilloscopes
- D9030DDRC DDR3 and LPDDR3 Compliance Test Application for Infiniium Series oscilloscopes
- U4164A logic analyzer system or 16864A benchtop logic analyzer
- Logic analyzer software B4661A, B4661A-1FP / 1TP / 1NP, B4661A-3FP / 3TP / 3NP, B4661A-4FP / 4TP / 4NP

DDR2

- UXR-Series oscilloscope
- DDR2 and LPDDR2 Compliance Test Application for Infiniium Series oscilloscopes
- U4164A logic analyzer system or 16864A benchtop logic analyzer
- B4661A, B4661A-1FP / 1TP / 1NP, B4661A-3FP / 3TP / 3NP